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A High-Performance Environment for Modelling and Simulation of Digital Systems

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Abstract

Today, digital system designers in the communication's industry need a variety of tools, sometimes manufactured by different vendors, to design their complex digital circuits. This paper describes a new design tool that integrates accurate time-domain measurement tools, with reliable modeling tools, and fast simulation tools into one complete solution that can simulate entire digital systems which can include active components, transmission lines, connectors, etc.

Authors

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Current Activities:
Silvio Forno is the software development manager of HDT. His particular areas of interest include device modelling and electronic CAD. He is currently involved in design and development of HDT products.

Author Background:
Silvio received the engineer degree (Dr. Ing.) from the Politecnico di Torino, in 1987 and Ph.D. in Computer Science in 1991. He joined HDT in 1991 after having spent the last three years in Computer Science Department of Politecnico di Torino working on telecommunication system simulation and real time systems.

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Alberto Biondello

Current Activities:
Alberto Biondello is a member of the HDT customer support team. He works on passive and active device modelling and post-layout simulation of digital systems.

Author Background:
Alberto received the engineer degree (Dr. Ing.) in electronics from the Politecnico di Torino, in 1992, after 1 year stage at Olivetti, working on signal integrity issues in high-speed computers.

Viscardo Costa

Current Activities:
Viscardo Costa is responsible for EMC Physical Design in the Electronic Switching Division, R&D, of Italtel. His particular areas of interest include EMC design for EMI control in digital systems, and CAD and device modelling.

Author Background:
Viscardo received the engineering degree (Dr. Ing) from the Politecnico di Milano in 1986. He joined Italtel in 1986 where he has been involved in various aspects of EMC phenomena in digital circuits, semiconductor development and interconnections effects in high-speed ICs. He has published several papers on Computer Aided Design, Device Modelling and models to analyze EM emissions, susceptibility, and crosstalk for PCBs and cables.

Slide #1

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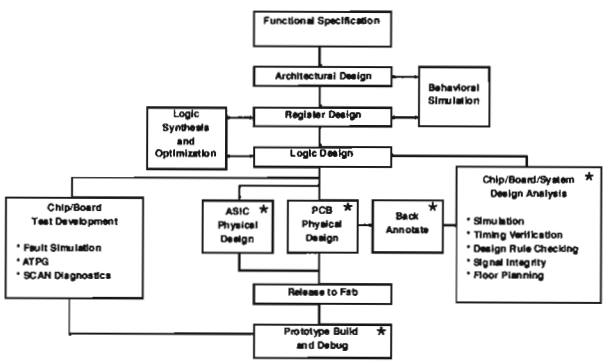
Slide #2

Simplified HS Digital Design Process



Slide #3

Overview

- Emerging hardware requirements for TELECOM
- TDR/TDT measurements and behavioural time modelling
- Case study #1: High-speed PCB interconnect
- Case study #2: Pre-layout design of ATM switch interconnects
- Complex system design & validation examples
- The new modelling & simulation environment
- Post-layout quality check

Slide #4

Evolution of Telecom Systems

- Transmission standards
  - SONET
  - SDH (155 Mbit/s - 2.4 Gbit/s)
- Switching systems for BISDN
  - STM/ATM crossconnects
  - STM/ATM switches
- High-speed LAN MAN
- GSM
- HDTV
- High-density component technology
  - Fine pitch
  - MCM

The fast evolution of telecom systems, the related emerging transmission standards and the new switching system architectures push toward higher operation speeds.

The Synchronous Optical NETwork (SONET) and the SDH standards require operating speed ranging from 155 Mbit/s (STM1) up to 2.4 Gbit/s (STM16). Broadband switches and crossconnects operating in STM (Synchronous Transfer Mode) or ATM (Asynchronous Transfer Mode) must be able to deal with these high-speed digital streams. On the other hand, the scaling down of integrated circuits and the high-density packaging and interconnection technologies like MCM (MultiChip Modules) give telecom manufacturers new opportunities to develop low to medium speed applications where miniaturisation, power dissipation, and reliability are key problems to solve. GSM (Groupe Speciale Mobile) terminals are a typical example of this kind of application.

All these new performance and quality requirements have a great impact on system design and test.

Slide #5

New Performance & Quality Issues

Signal integrity

Timing & synchronization

EMC/EMI

Hardware designers and validators have to face a new set of constraints. First of all, good signal integrity becomes a major goal, not only at transmission interfaces, but everywhere in the system. Issues like signal reflections, crosstalk, and switching noise must be controlled and kept below assigned thresholds at the various interconnection levels of telecom apparatus. Timing distribution and synchronisation also play a fundamental role in overall system robustness. ElectroMagnetic Compatibility (EMC) and ElectroMagnetic Interference (EMI) issues must also be considered because systems must comply with the relevant international standard. New design and test tools are needed to help system designers and validators solve these tough problems.

Slide #6

The Ideal Design & Test Toolset

- Wideband characterisation
- Fast & accurate modelling
- Fast & accurate simulation
- Telecom-oriented test procedures
- Full integration of previous items

The ideal tool set would require some important features. First of all, the capability of making fast and accurate characterisations of devices and subsystems with a time resolution compatible with the actual application bandwidth is important. Accurate models would be extracted quickly from these experimental characterisations to perform high-fidelity simulations. The simulation engine would support high-complexity situations, typical of telecom apparatus at various levels, such as electrical, behavioural, timing, in order to quickly perform pre- and post-layout analysis of subsystems. The capability of simultaneously taking into account several effects like signal reflection, crosstalk, switching noise, timing skews and logic behaviour is very important in system quality analysis. Moreover, telecom applications require new checks and procedures like eye diagrams, signal compliance analysis, and test pattern generation for performance verification. A strong integration of experimental characterisation, modelling techniques, simulation, and system testing is fundamental to fully achieve performance and quality goals of telecom apparatus.

Slide #7

Limitations of Many Conventional Simulation Tools for HSD Circuits

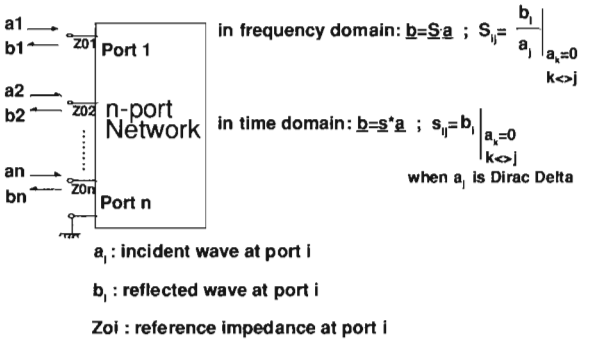
- Slow and difficult modelling procedures
- Slow & limited simulation engines for HSD designs
- Poor integration with experimental measurement

HSD = High Speed Digital

This paper will present a new set of experimental/ simulative tools that overcome all the limitations of conventional tools. These new tools have strong integration with wideband test and measurement instruments, so that accurate electrical models are easily extracted. A telecom apparatus is simulated without any problem of convergence and speed, even in those complex situations (ones with tens of thousands of circuit elements are common nowadays) where, until now, it was not possible to perform even a simple analysis, especially when transmission line analysis is required.

Slide #8

S-parameters Representation of Networks



The scattering, or S-parameter family is defined to relate incoming and outgoing waves at the ports of a network. In general, an n-port network has n^2 S-parameters associated, with n port reference impedances, Zoi , i = 1, 2, ..., n. A single reference impedance, Zo, is usually chosen for all ports. For a linear n-port network, the defining equation at a given frequency is:

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

where a_i represents the incident wave and b_i the reflected wave at port i. The frequency domain S-parameters can be interpreted as reflection (S_{ii}) or transmission (S_{ij} , i<>j) coefficients in matched conditions. They are, in general, complex numbers and their use is well known in microwave applications.

In the time domain, a convolution relationship applies:

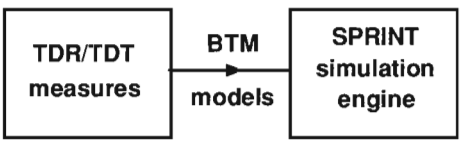
$$b_1 = s_{11}*a_1 + s_{12}*a_2$$

$$b_2 = s_{21}*a_1 + s_{22}*a_2$$

where s_{ij} is the generic reflected or transmitted wave in matched conditions when the incident wave is a Dirac Delta .

Slide #9

A New Approach to Modelling: BTM



A new modelling technique called BTM (Behavioural Time Modelling) is introduced. It is based on the fact that time-domain characterisation of components is the most straightforward and realistic way to get models in high-speed digital applications. Wideband TDR/TDT instruments, like those made by the HP 54120-series, are the optimal solution to perform this task, even if conventionally, they are utilised predominantly as verification tools. In fact TDR/TDT analysis of a fully terminated n-port device configuration corresponds to the measurement of the S-parameter step-response in time domain. The accuracy is good for digital applications because of the extreme precision of the TDR pulse, with amplitude aberration with respect to the ideal step limited to less than 1%. BTM directly utilises these S-parameter responses to extract models of the Device Under Test (DUT). Models obtained in this way are also suitable for most EMC/EMI applications. These wideband models can be validated by simulating the TDR/TDT set-up and comparing the simulated responses with the actual measurements.

The simulated responses of target systems, containing the modelled devices, can be also compared with the actual system measurements, performed with the same HP 54120 used as a wideband sampling oscilloscope, where the instrument's 50-GHz bandwidth helps to give extremely high confidence in the verified model. The overall procedure requires strong integration between the measurement and simulation environments.

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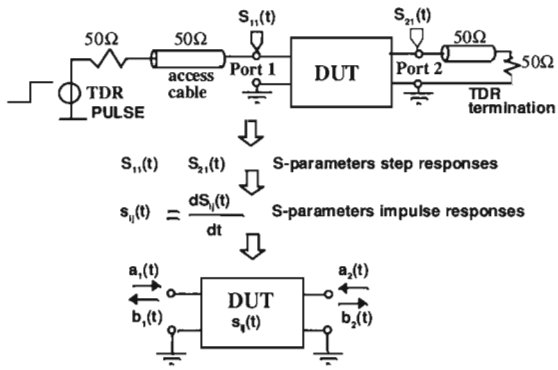
Slide #10

2-Port DUT as BTM Black Box



Using BTM, the DUT is considered a "black box", accessible only through its ports. For instance, a 2-port linear device is fully characterised by its four S-parameter step responses: $S_{11}(t)$, $S_{12}(t)$, $S_{21}(t)$, $S_{22}(t)$. The device is reciprocal if, $S_{12}(t) = S_{21}(t)$. In the case of a symmetrical 2-port device, $S_{11}(t) = S_{22}(t)$. Symmetrical and reciprocal 2-port devices require only two S-parameter behaviour models. S-parameters impulse responses, $s_{ij}(t)$, are easily calculated as time-derivatives of step responses, $S_{ij}(t)$. When the DUT is connected to an external network, the following relationship applies between reflected waves, b, and incident waves, a, at its ports:

$$b_1(t) = s_{11}(t) * a_1(t) + s_{12}(t) * a_2(t)$$

$$b_2(t) = s_{21}(t) * a_1(t) + s_{22}(t) * a_2(t),$$

where the symbol "*" denotes the time convolution operator.

Slide #11

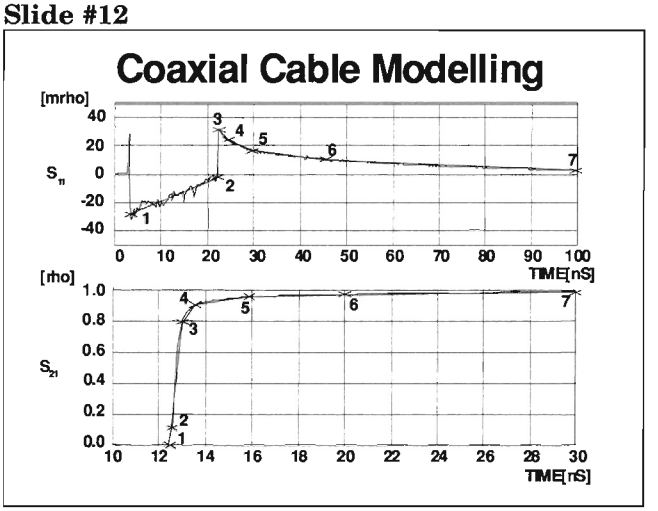
PWL Fitting of BTM : Benefits

- **Only few breakpoints normally required**
- **Speed up of simulation runs**
- **Purely ohmic non-linear behaviour added to dynamic response**
- **Good for EMC/EMI models**

Time domain simulations require time convolutions to calculate port signals when the BTM model is connected to an external network. A PWL (Piece Wise Linear) fitting of mentioned S-parameters can dramatically speed up this convolution process. As it will be shown in the following, for most situations only a few breakpoints are normally required to describe S-parameter behaviour, taking into account the accuracy constraints of digital applications (order of some %). This PWL fitting procedure is fully supported by the MCS (Model Capture System) of the graphical environment.

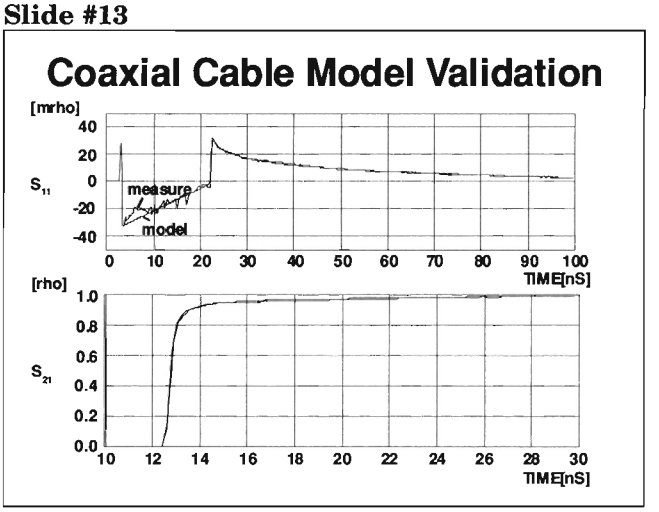
Another important consideration is that non-linear effects of I/O ports of digital devices (ICs) can be modelled with good approximation as purely static (ohmic) non-linearities, superimposed to a linear dynamic response. Simple examples will explain in further detail how to utilise this modelling technique in high speed digital design.

Slide #12



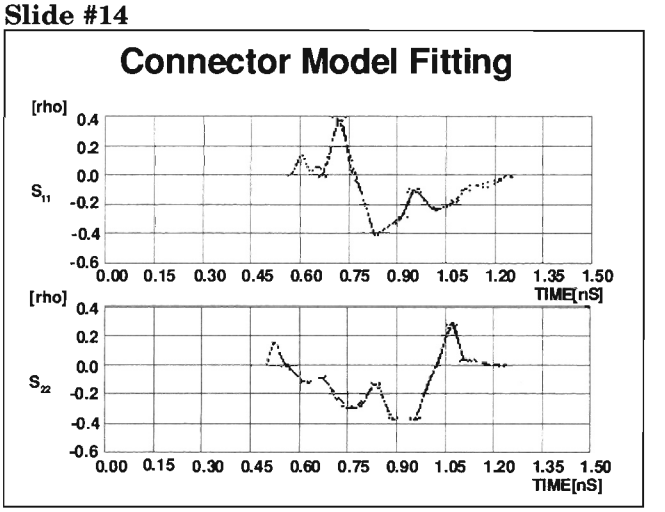
The slide shows the S_{11} and S_{21} characterisation of a microcoaxial cable 2 meters long and its related PWL fitting with 7 samples. Skin effects are clearly visible. In this case, the model is directly implemented by a 2-port block whose S-parameters are described by the PWL behaviour extracted from TDR/TDT measurements. To achieve a good model accuracy, it is important to activate the built-in normalisation algorithm provided by HP 54120 TDR before starting the characterisation process. This procedure will ensure the exact calibration of both time and amplitude (mrho) scales.

Slide #13



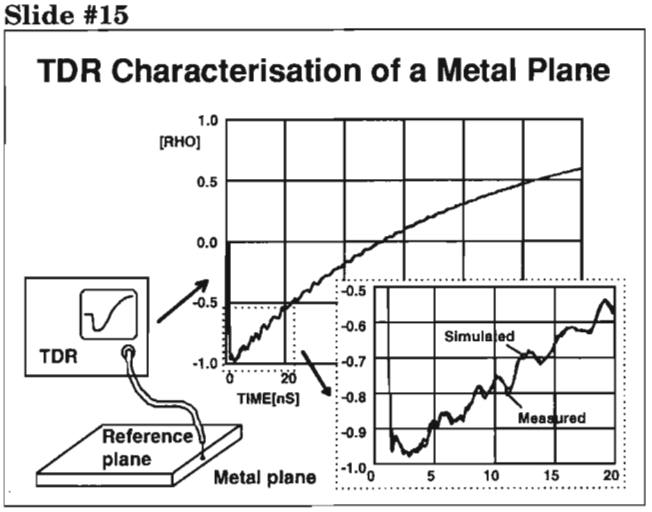
The behavioural model can be validated through a simulation of the measurement set-up, in which a voltage generator (with 50-ohm internal impedance) sends a fast edge (as well as the TDR does) to the modelled cable. This slide shows the correspondence between the simulated response versus the actual measurement (also shown on the figure). In this simple case, the model response is an exact replica of the PWL behaviour previously extracted. Skin effects and dispersion are accurately modelled, avoiding analytical efforts. The models can be used in chains or subcircuits for modelling longer sections of cable.

Slide #14



The methodology can also be applied to model asymmetrical devices (for example connectors), whose structures are very difficult to treat in terms of lumped parameters because of their discontinuities. A Behavioural model is more accurate and easier to build. In this case, 3 S-parameters (S_{11}, S_{21}, S_{22}) need to be known because the device is not symmetrical. The slide shows the reflectometer response for S_{11} and S_{22} and related PWL fitting of a PCB connector. The fitting starts after the first peak, which is the parasitic effect due to the launch cable, to the point where it is joined with the device under test. This portion of the response can be ignored.

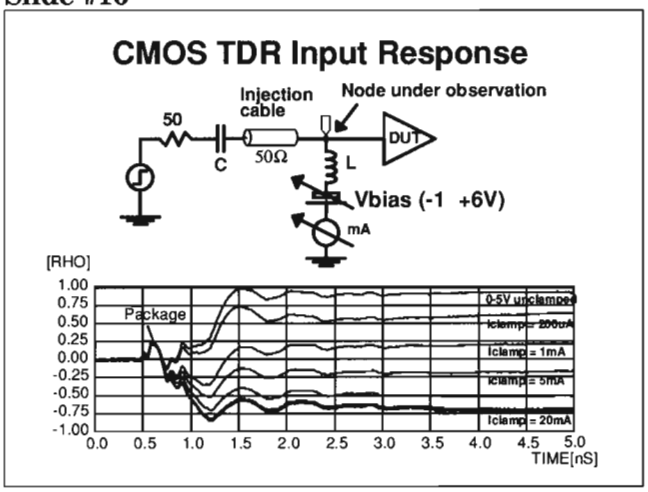
Slide #15



For fast edge operation, the power and ground distribution planes cannot be considered ideal. In fact, the current injected in a particular point of the plane (for example, by a switching driver or a termination) and its propagating phenomena cause noise that can affect other devices placed on the same substrate. Using a mesh of behavioural blocks, it is possible to build up two dimensional models of power and ground planes and take this effect into account. The TDR is an excellent vehicle of validation of this model.

The slide shows the comparison between the TDR measurement of a two-layer metal plane (the second plane acts as reference plane) and a simulation of the model in the same configuration. The global behaviour is roughly the typical reflectometer response of a capacitor. A detail of the first section of the graph shows the reflections of the TDR step due to the plane boundaries. It is interesting to point out the very good matching between measured and simulated results. Changing the signal injection point causes a strong modification of these reflections. Accurate ground and power plane modelling is fundamental to simulate the residual switching noise on multilayer PCBs or MCMs taking the effect of decoupling capacitors into account. Model parameters are optimized through a trial and error technique comparing the actual measured response with the simulated TDR response of the model. This process is fast due to short simulation time required.

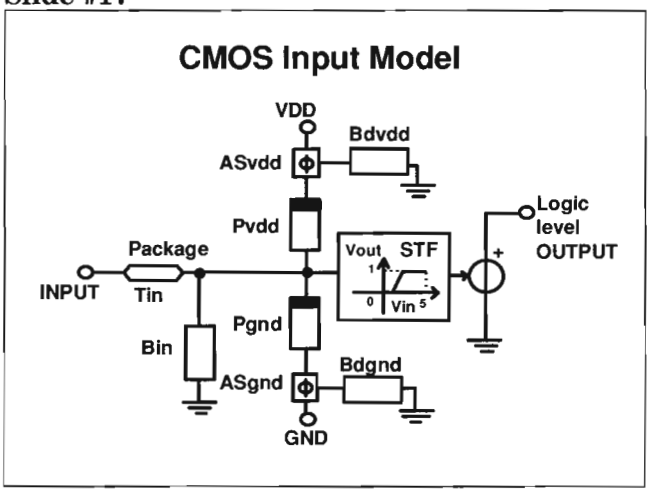
Slide #16



The BTM methodology described before for passive components applies as well for the modelling of the I/O interfaces of active parts. Using the TDR, it is possible to create an accurate model of the dynamic behaviour of an input or output in both normal operating conditions (within the logic swing) or non-normal conditions, such as, in clamping situations, including the package effect (lossy or lossless). Other modelling approaches (as simple Thevenin equivalents) are inaccurate or too slow (for example, SPICE MODEL cards) to be used for the simulations of large systems.

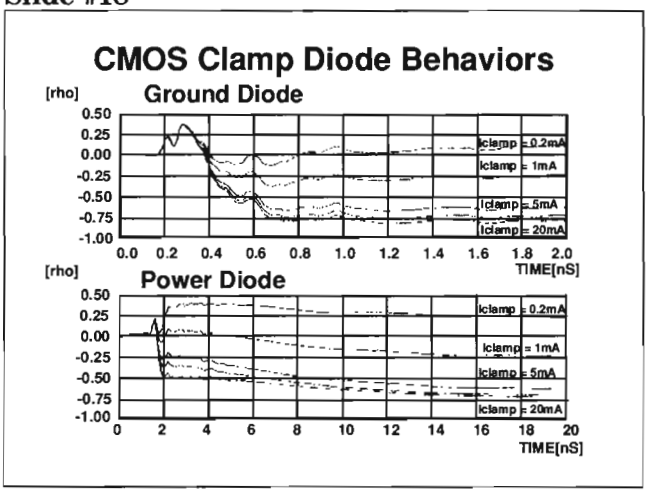
The measurement setup consists of a HP 54121T TDR and a bias generator. The 200mV step provided by the TDR pulse generator can be considered a small amplitude signal compared with the 5 V swing of CMOS output levels. A X10 matched attenuator, connected at the pulse generator output, will provide a "small" amplitude stimulus (20 mV) for low swing devices (such as, ECL). The inductor, L, has been inserted in order to present a high impedance path to the TDR pulse on the biasing stub. The capacitor, C, acts as a DC block in order to avoid injections of direct current into the TDR pulse generator and is practically a short circuit in the time window of the measurement. Obviously both L and C must have low parasitics in the frequency range of interest. Anyway, their non-ideal effects can be taken into account during simulation and model validation, effectively removing their effect by normalisation.

Slide #17



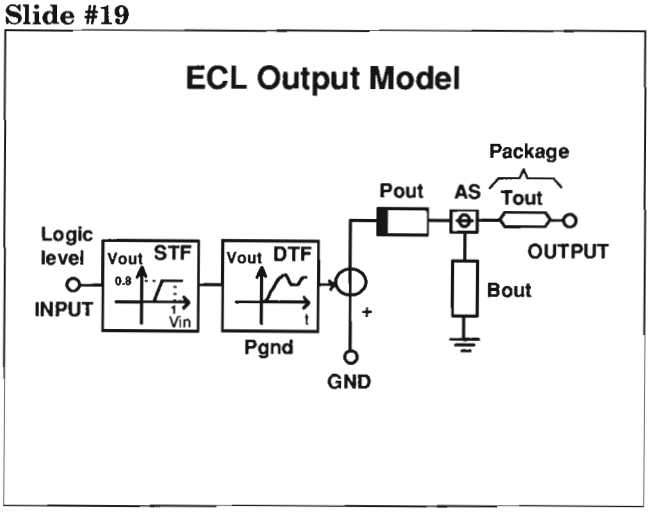
Few model architectures can represent all the major component families. For example, this slide shows a typical CMOS input model. The static characteristic is modelled for both the clamping diodes (Pvdd and Pgnd) and can be obtained by a V/I measurement, while the dynamic behaviour of the clamping diodes and the input in normal conditions is measured using the TDR. The Bin, Bdvdd, and Bdgnd elements are described directly by measured samples or by their PWL fitting. The Bin block models the input of the device when both clamping diodes are off. The Series Adaptor blocks, ASvdd and ASgnd, are utilized to connect the behavioural blocks, Bdvdd and Bdgnd, which take package effects into account, in series to power and ground nets, respectively. The Static Transfer Function (STF) can be utilised to convert the external analog levels to internal digital ("0", "1") levels. A set of library functions (AND, OR, etc.) can model internal logic and timing behaviour.

Slide #18



The slide shows two families of reflectometer responses related to power and ground clamping diodes versus clamping current of a CMOS EPROM input. It is interesting to point out the different behaviour of the two diodes. The ground diode shows a very fast response, so that low impedance levels are reached in about one nanosecond. On the contrary, the Vdd diode shows a slow transient (several nanoseconds long) before it reaches low impedance levels.

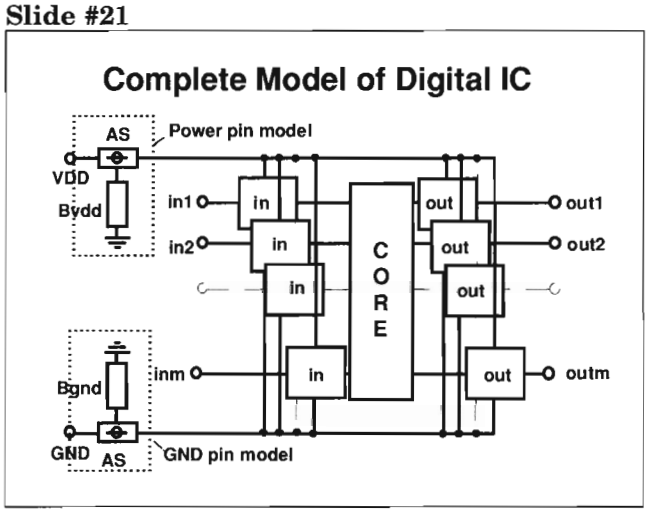
Slide #19



An ECL device presents a strong output resistance non-linearity at low current loads. During the falling transition, there are situations where the

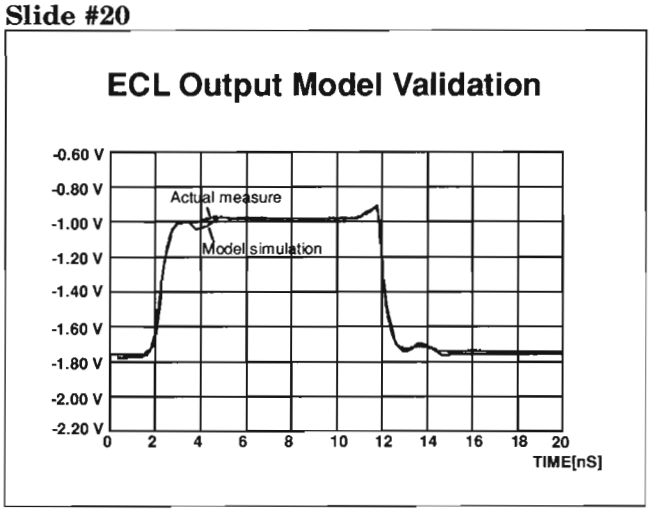
output transistor goes near cutoff and its output impedance greatly increases. The reflection coefficient's dynamic behaviour (Bout) is usually the same for both "0" or "1" logic states, as well as the static output characteristic (Pout). The near inductive TDR response of the output emitter follower is modelled by the Bout block series connected through the series adaptor, AS. The Static Transfer Function (STF) translates the internal logic levels, "0" and "1", to output electrical levels, while the Dynamic Transfer Function (DTF), measured by a a digital sampling oscilloscope, shapes the output waveform behaviour.

Slide #21



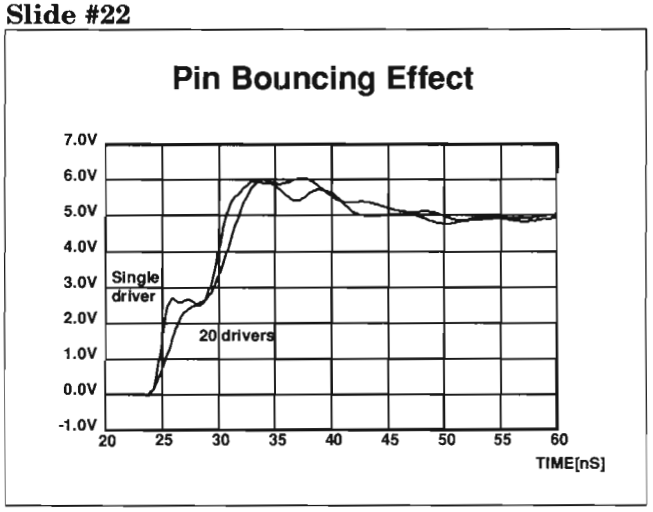
All the previously mentioned models can be combined to build up a macromodel of an entire device composed of an input section, output section, a core section (at logical levels describing the logic/ timing function of the device), and a behavioural model of power and ground pins created by means of TDR measurements. This model can also be used for an accurate simulation of the simultaneous switching noise, because all the input and output pins are coupled together by common power pins.

Slide #20



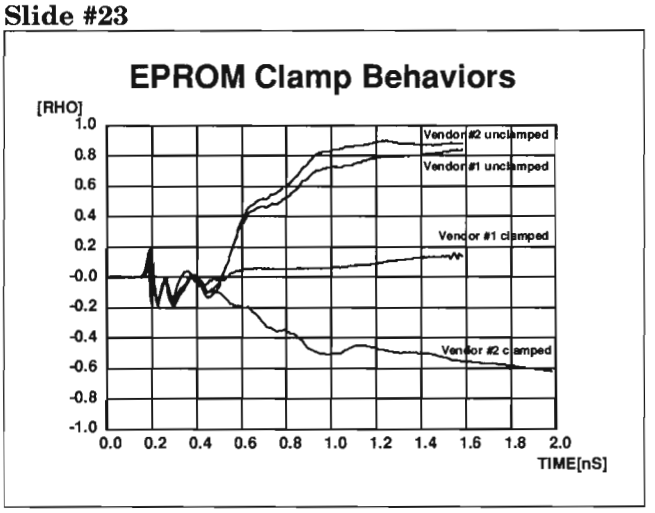
A model of an ECL output of a BiCMOS ASIC is validated by comparison with the actual measurement. The output load is 50 ohm to -2 V, so that all the elements of the model, shown in the previous slide, concur to determine the resulting waveshape.

Slide #22



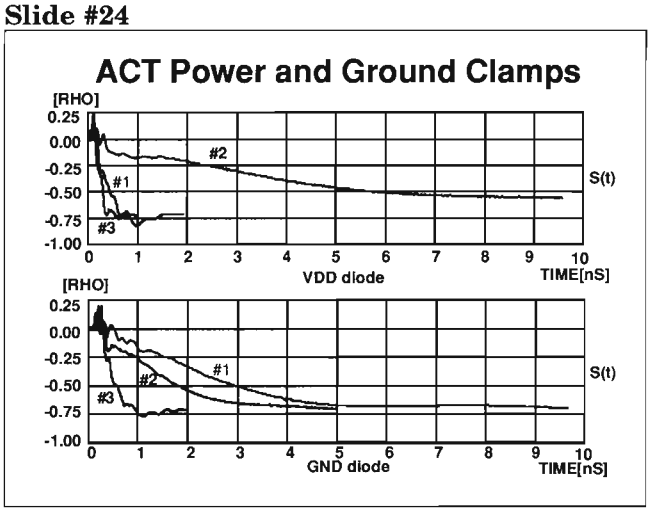
This slide shows the comparison between two simulations of an actual PCB interconnect with and without Pin Bounce effects. The driver's package contains 20 CMOS outputs driving 5 input loads each. The driver's model is of the type shown in the previous slide, where package coupling is modelled by behavioural blocks, Bvdd and Bgnd, obtained from TDR measurements on power and ground pins, respectively. In this case, the pin bounce determines a slow down of waveforms at receivers because the outputs switch simultaneously in the same direction. In a more general situation with random rise and fall transitions, a jitter effect would appear at these receivers. The amount of pin bounce strongly depends also on power and ground distribution nets, so that accurate models of them are needed.

Slide #23



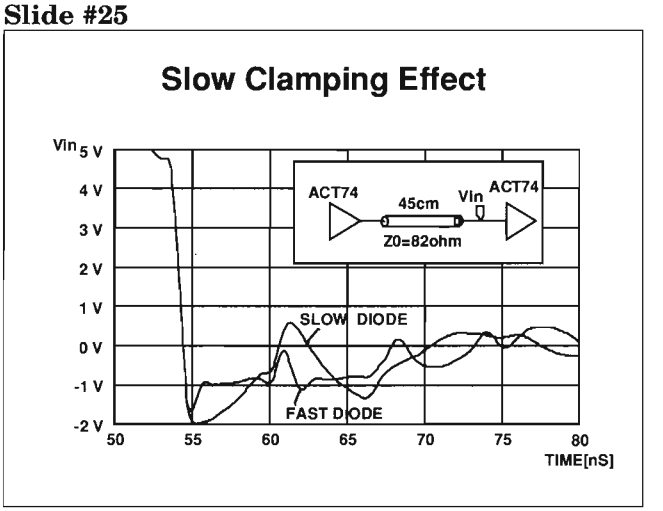
The same TDR measurements performed on input or output pins of active parts for modelling purpose can also be used during incoming test, in order to check the quality of the component. In fact, the same device produced by different foundries could present completely different dynamic behaviours. The slide shows the TDR responses of the inputs of EPROMS (27C512) supplied by two different vendors. It is possible to point out the different behaviour in clamp condition (15 mA of direct current is flowing in the diode), while in normal condition (within logic swing) the behaviour is similar.

Slide #24



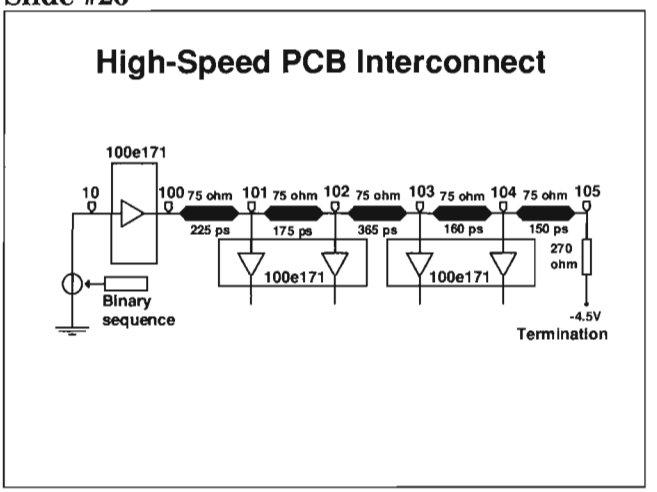
The slide shows the dynamic behaviours of ACT74 input diodes in clamping condition (20 mA direct current). It is interesting to point out that the vendor #2 part presents the slower dynamic behaviour for power diode and a relatively fast response for ground diode. While the vendor #1 part presents a fully reversed behavior of its clamps. This example confirms how this kind of characterisation is necessary to get reliable simulation results.

Slide #25



This slow behaviour has a great impact on the clamp action, so that if a voltage overshoot, due to reflection occurs, it will be effectively clamped only after the delay observed in the TDR characterisation. Due to the difficulties to forecast these effects, only this modelling approach, based on experimental measurements, can accurately take all the effects into account. The slide compares the simulation of a point-to-point interconnection 45 cm long using an ACT74 as receiver with the same static characteristic but different dynamic behaviour in clamping condition (vendor #1 and #2).

Slide #26

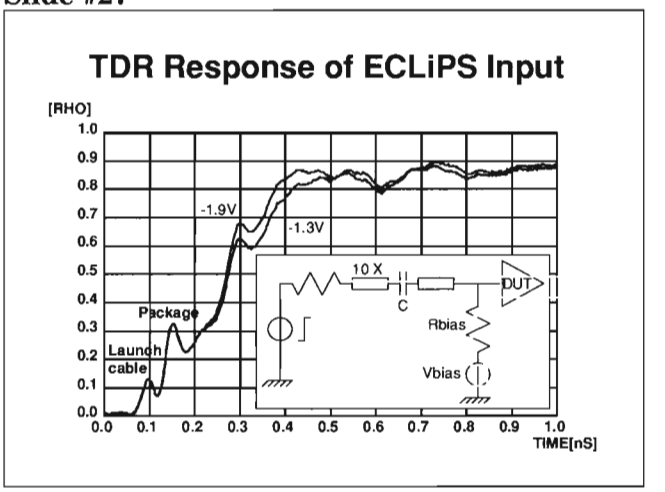


A PCB (Printed Circuit Board) interconnection among subnanosecond ECL (ECLiPS) devices has been utilised as simple example to show a typical high-speed design application.

The situation shown consists of an ECLiPS 100e171 multiplexer driving 4 receivers connected to a PCB bus. The receivers belong to two separate packages. All drivers are packaged in plastic chip carriers (20 pin PLCC) and are connected to the breadboard by sockets. The input stimulus can be generated internally by means of a simple loop oscillator, generating a 192 MHz clock signal, or externally by means of a high-speed pattern generator. The bus termination consists of a single pull-down resistor connected to VEE supply (-4.5 V), or a Thevenin termination. The single pull-down leads to an unterminated situation that has been analysed in order to check the effectiveness of the method, even in marginal operating conditions.

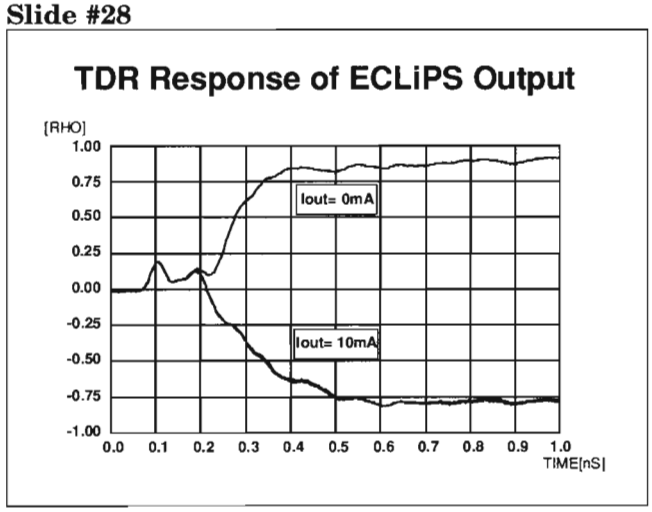
This example is used in the demonstration case study.

Slide #27



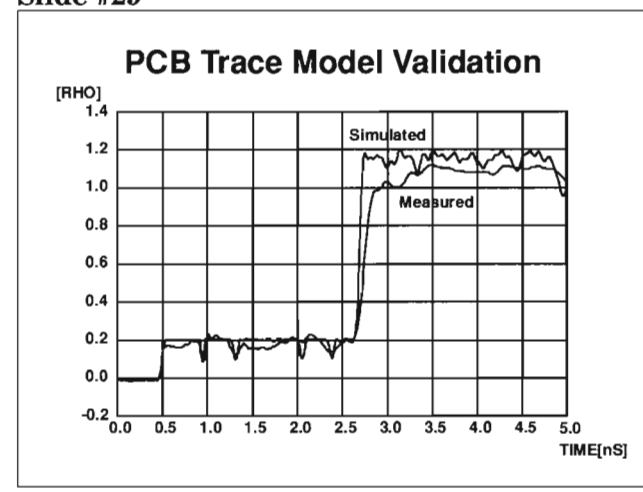
Shown is the behaviour of the measured reflection coefficient of a socketed 100e171 input (pin 6) at two biasing levels (-1.9 V corresponding to a logic "0" level and -1.3 V corresponding to VBB). These two responses are slightly different because at VBB the input draws current. The effects of launch cable and package assembly are clearly visible. It is easy to separate packaging effects from the active input contribution because the package response is independent of the bias levels. The resistive effect of biasing network (Rbias) is also visible because the asymptotic value of the input reflection coefficient is lower than 1. This effect can be cancelled by resimulating the setup connecting a negative resistance (-Rbias) in parallel to the behavioural block described directly by the acquired samples. From this new response a BTM model is extracted using a PWL fitting.

Slide #28



The output reflection coefficient of an unsocketed 100e171 is measured at several bias conditions. If the output current is constant (10 mA), the behaviour at both logic levels are practically the same. At 0-mA current, the emitter follower output shows a high-impedance to the TDR pulse. Launch cable connection and packaging effects are again clearly visible, because they do not depend on bias levels and these effects can be discarded when the model is built up. Output rise and fall edges, at constant current (10 mA), are also acquired because they practically represent the output model waveshape in unloaded conditions. Both input and output models are completed adding their non-linear static characteristics, modelled by a PWL resistor. The pairs of values (v, i) can be obtained by an automated power supply and precision digital multimeter setup.

Slide #29



A simple lossless model of interconnecting traces, including the short stubs toward receivers, is obtained extracting geometrical data from board layout. The microstrip delays and impedances are calculated starting from crossection data through standard formulas. This slide shows the TDR model response of the trace left open without the device connected, compared with the actual response. There is a good match regarding delays of various trace pieces. Some impedance discontinuities due to geometrical changes in the crossection are present, even if the average impedance level is in good agreement with theoretical value. Skin effect losses cause the typical slow down (about 80 ps) of TDR edge reflected by the open end of the interconnect. This lossless transmission line model can be utilised for preliminary interconnect simulations. A more realistic model can be obtained substituting lossless lines with lossy lines, modelled as 2-port S-parameter blocks with the BTM technique.

Slide #30

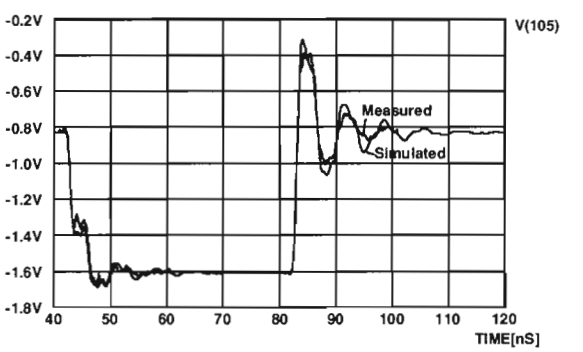
Interconnection Netlist

```
**********************************************************
INTERCONNECTION DESCRIPTION
XDR 10 100 DRE171
T1 100 101 Z0=75 TD=225PS
XREC1 101 RCE171P
T2 101 102 Z0=75 TD=175PS
XREC2 102 RCE171P
T3 102 103 Z0=75 TD=365PS
XREC3 103 RCE171P
T4 103 104 Z0=75 TD=160PS
XREC4 104 RCE171P
T5 104 105 Z0=75 TD=150PS
* pull-down resistor
VTERM 105 0 DC(-4.5V) 560
* edges
VIN 10 0 PULSE(1 0 40N 0 0 40N 80N) PSEQ (10100010111110000011111000)
.OPTIONS  DELAYMETH=INTERPOLATION
**********************************************************
.TRAN TSTART=40N TSTEP=10PS TSTOP=120NS LIMPTS=1000 V(100) V(101) V(102)
V(103) V(104)
+ V(105) I(T1,100)
.END
```

The simulation's netlist of the whole interconnection network is shown in the slide. Driver and receiver models are described as SPICE-like subcircuits. The driver model includes an input port that only has logical meaning when using 0 V and 1 V as input levels. This feature is very useful to define stimuli composed of sequence of "0" and "1", identified by PSEQ keyword in the PULSE statement extension of the simulator.

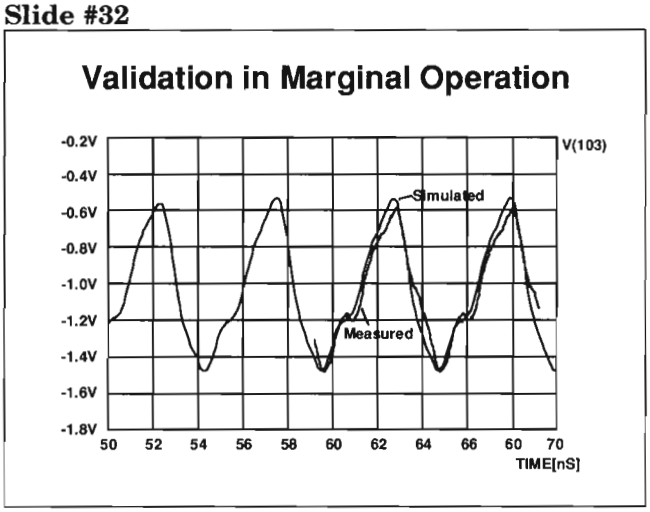
Slide #31

Rise and Fall Edge Shapes



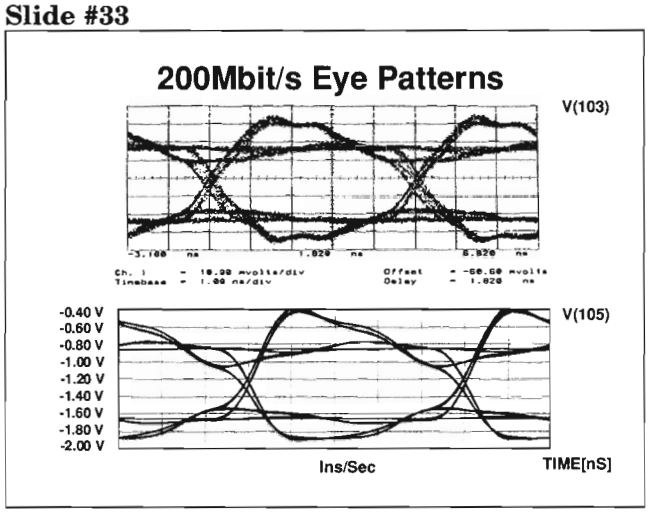
The whole interconnection model has been simulated for various termination values. A typical simulation run requires about 1.5 s on a HP 750 workstation. As shown in the slide, a 560 ohm to -4.5 V termination causes a strong difference between falling and rising edges at the receivers. The falling pedestal edge is affected by a round-trip delay at -1.4 V, due to output transistor cut off, while the rising edge is followed by a great amount of ringing due to termination mismatch. Using a 270 ohm to -4.5 V termination, the operation becomes quasi-linear, so that the -1.4 V pedestal disappears, but both edges are followed by a consistent amount of ringing due to termination mismatch. To verify the accuracy of the models and the simulation, a comparison with measurements is performed on the actual breadboard using the HP 54120 digital oscilloscope. The results obtained are shown in this slide, where it is possible to point out the good match between measurement and simulation, even in these critical functioning situations.

Slide #32



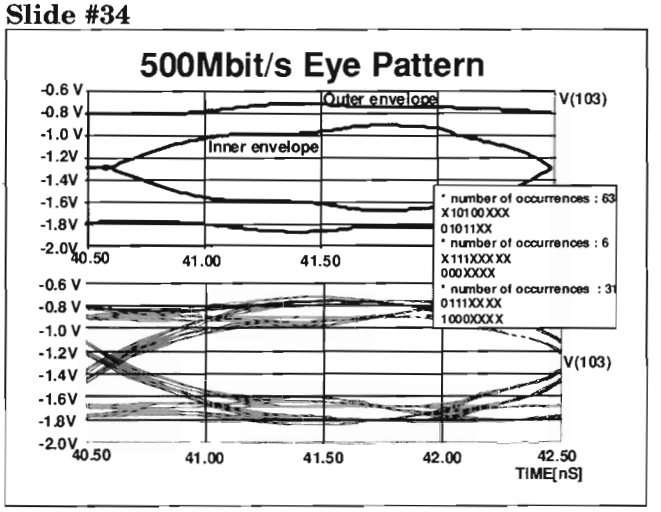
This slide shows a comparison between the measurement and the simulation when a 560 ohm termination and an input stimulus of an 192 MHz 0101 ..... sequence, obtained from the internal oscillator, is used. In this non-linear situation, the edge difference and interaction cause a strong shift towards ground of the waveform swing, so that the waveshape is completely unacceptable. Even in this critical situation, the match with actual measurement still remains good.

Slide #33



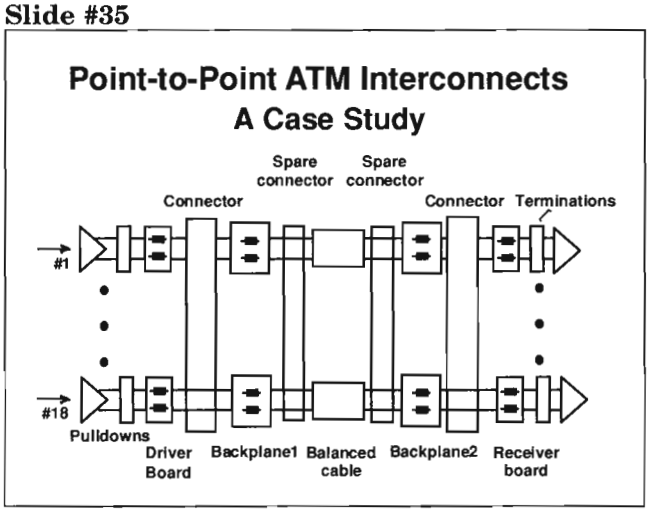
To obtain better operation, a lower termination value (270 ohm to -4.5 V) is evaluated. Measured and simulated eye diagrams at the input of third 100e171 input (V(103)) are compared in this slide. The input stimulus is an 63-bit NRZ Pseudo Random Binary Sequence (PRBS) at a 200 Mbit/s data rate. The dissymmetry affecting the eye's outer shape, due to the non perfectly linear driver operation, caused by the still high termination value, is still evident.

Slide #34



A higher speed (500 Mbit/s) operation is analysed with the interconnection terminated in a 75 ohm to -2.5 V Thevenin equivalent. In this case, the driver operation is linear, so that the eye pattern diagram can be used to determine the worst-case pattern that is causing the maximum eye closure at 500 Mbit/s. This pattern is then used as input stimulus for both interconnect model and actual breadboard. In this last case, the worst-case sequence is loaded on the high-speed pattern generator, such as the HP 80000A data generator system and injected at 500 Mbit/s at the input of driving 100e171. The eye diagram is compared with simulated eye diagram in this slide. The eye diagram mask facility is very useful to quickly evaluate the digital bandwidth of a system, starting from its simulated or measured step response.

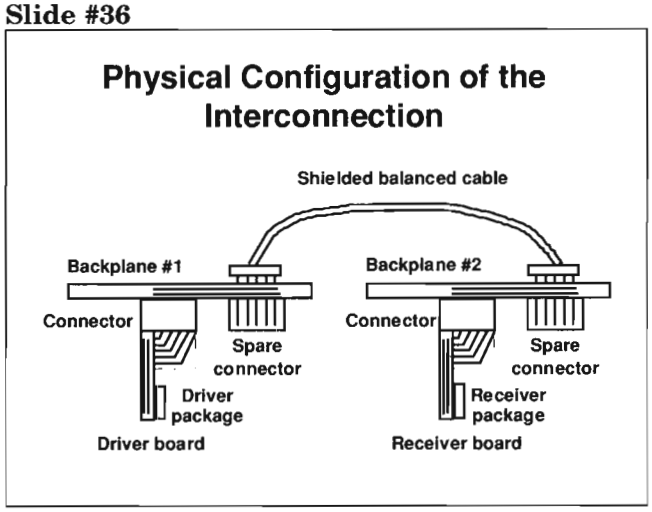
Slide #35



In telecom design, pre-layout analysis plays a very important role because of the reduced noise and timing margins (skew, settling time, etc.). Pre-layout analysis should be considered very early during the design phase: in this way errors in the physical system architecture can be avoided; consequently, improving quality and reducing cost.

This slide depicts a point-to-point transmission for an ATM (Asynchronous Transfer Mode) cross-connect system. Inter-stage connections of a broadband cross-connect require throughput on the order of several Gbit/s. Given the number of signals involved, a model related to a three-link module (18 wire) can be developed to verify the overall noise coupling effects.

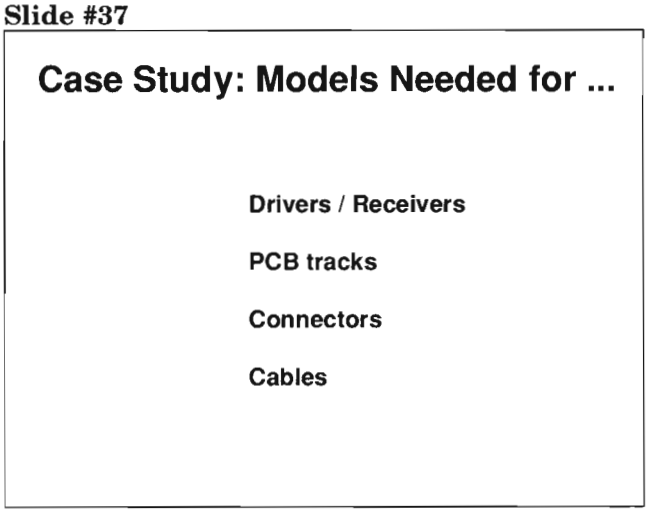
Slide #36



This slide shows the physical configuration of the interbackplane connection. Differential transmission was chosen to get the best result in terms of eye opening at the working bit-rate (155 Mbit/s). In fact, fully a balanced configuration ensures good common-mode rejection and minimises the effects of simultaneous switching noise.

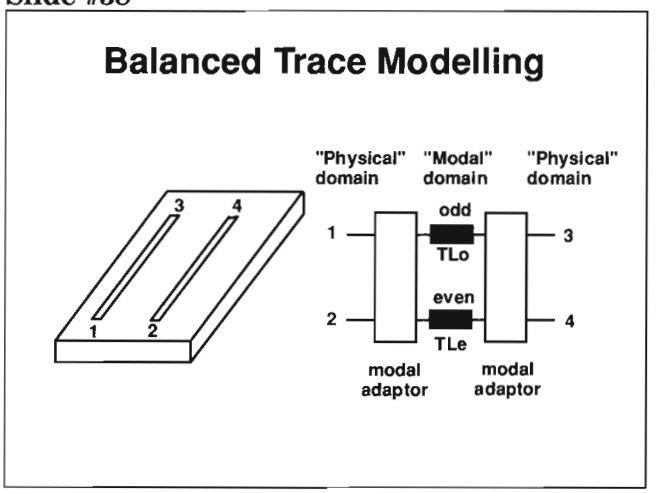
A shielded balanced cable of between 3 m and 9 m in length is used to connect the backplanes. A spare connector is provided to replace the electrical link with an optical one when the connection length is greater than 9 m.

Slide #37



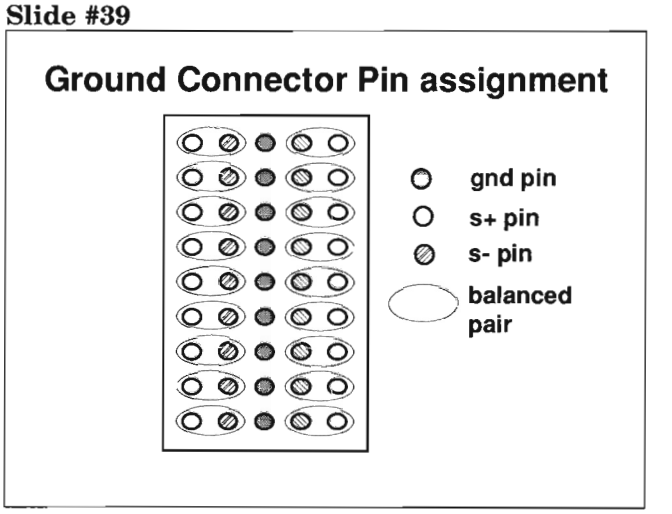
Several components have to be modelled in order to complete the simulation. Because active components (ECLiPS) have fast transition times (about 300ps), it is necessary to use very accurate time domain models of all component parts. Modelling techniques for ECLiPS components have been explained in the previous example.

Slide #38



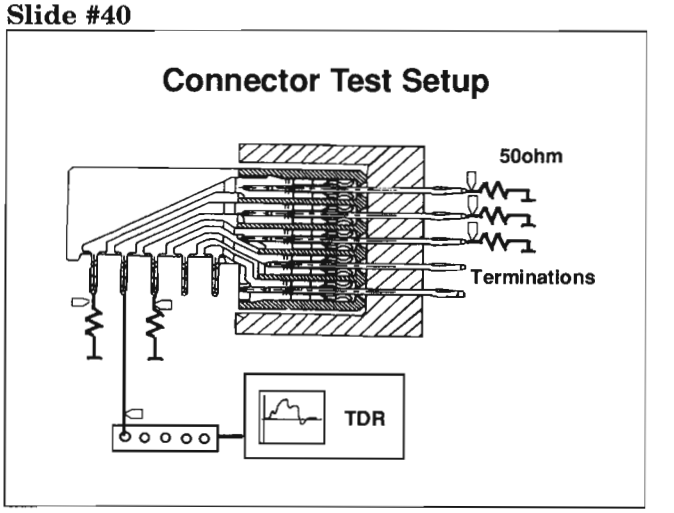
Each differential signal pair is carried by two coupled microstrips on the PCB. To model these traces, a transmission line model, based on modal analysis, is used. Two-mode decomposition is obtained using modal adaptor blocks. A modal adaptor converts physical waves of a multiconductor transmission line into modal waves according to the modal transformation, defined by its eigenvalues and eigenvectors. The simulator uses the modal adaptor as a primitive component. In the case of two coupled microstrips, only two modes (even and odd) are present. Transmission lines between modal adaptors represent even and odd mode propagation. Due to their short length (a few centimeters), you can assume these lines are lossless.

Slide #39



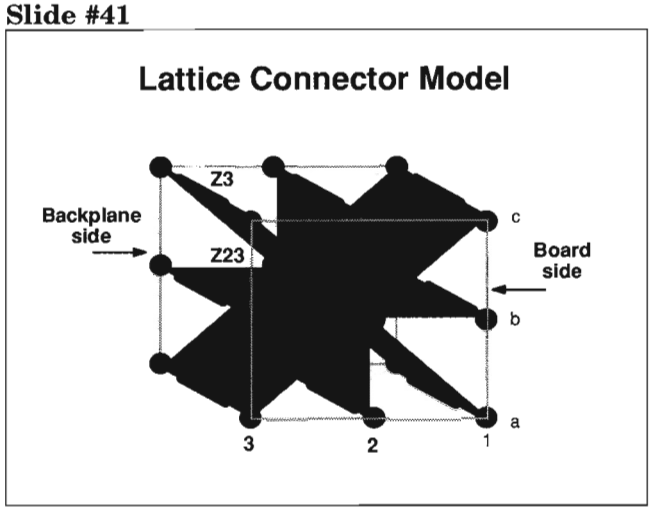
Considering the large number of signals and the use of balanced transmission, requiring two pins per link, a high-density PCB metric connector is usually chosen. It is necessary to position ground pins efficiently in order to preserve signal integrity with the minimum number of extra pins.

Slide #40



The first step is to build up an accurate connector model. A connector module of 9 rows and 5 columns is characterised by means of TDR/TDT techniques. Coupling voltages due to the TDR step are measured at adjacent pins. Direct coupling to non-adjacent pins is found to be negligible.

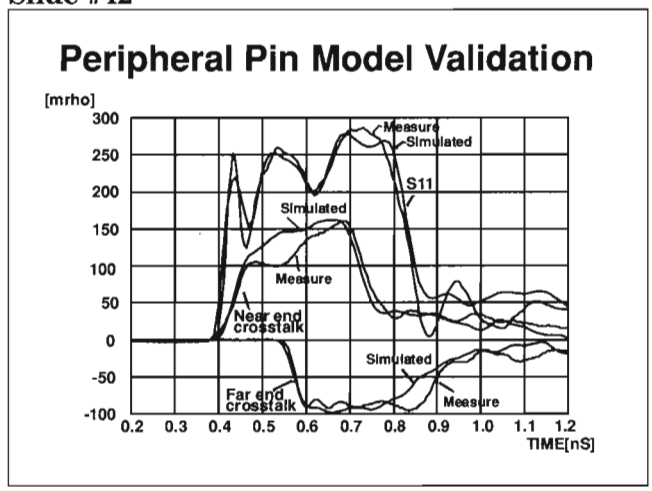
Slide #41



Starting from the previous statement, a lattice structure is selected to model the connector. Each pin has a direct coupling with adjacent pins. Due to fast operating edges and connector propagation delay (about 150 ps), a transmission line model (TLM) is the most suitable choice. This slide shows how this model couples each pin to its adjacent pins. The distributed intra-pin coupling is represented by a balanced transmission line while an unbalanced line models the coupling toward the reference ground plane.

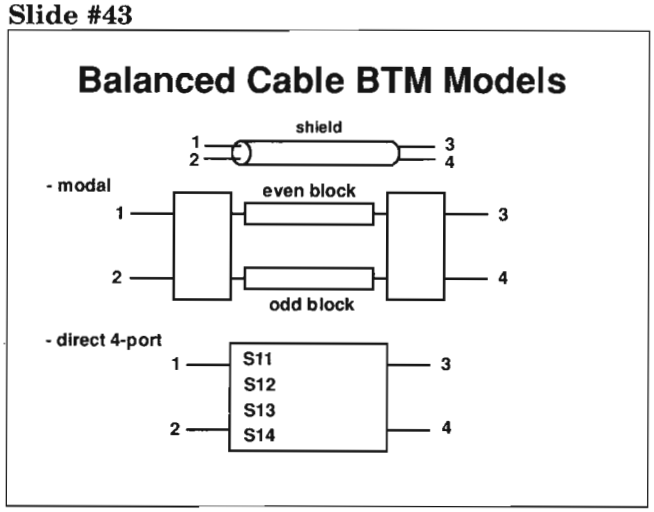
Using a trial and error fitting technique, the values of the model parameters are optimised through simulation of the experimental set-up. Despite the number of elements required to build up this 3-D model (about 700), the simulation runtime is very fast (about 2 seconds on an HP 750 workstation).

Slide #42



A comparison between measured and simulated TDR responses of two peripheral pins is shown in this slide. Transmission line effects are clearly visible, as is crosstalk behaviour. The lossless TLM models ensure good accuracy that cannot be achieved using conventional RLC models. A further accuracy enhancement can be obtained if lossless lines are replaced by lossy two-port S-parameters blocks.

Slide #43

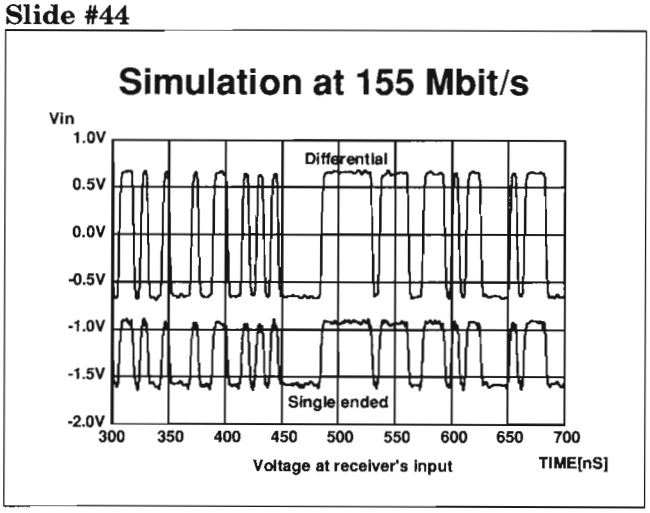


Because this application requires cable lengths of up to 9 m, cable models must include losses because they can have a significant impact on the fast signal edges (about 300 ps). The 4-port model of the balanced cable can be obtained in two ways. The first is through a modal decomposition, by means of two modal adaptors and two lossy lines representing even and odd propagation. Each line can be modelled using a PWL fitted 2-port S-parameter block.

Alternatively, a 4-port S-parameters block is used. Due to reciprocity and symmetry of the cable, only 4 different S-parameters are needed. This last model can be directly obtained from four unbalanced TDR/TDT measurements.

Both models are referred to the minimum interconnect length (3 m). Greater lengths (6-9 m) are obtained simply connecting two or three equal 3-m models in cascade configuration.

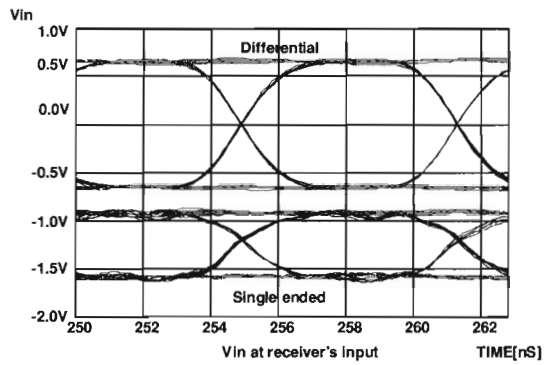
Slide #44



A complex model of the interconnection module (18 paths) is built up, in order to take all signal degradation effects into account. This model containing about 7,000 elements is stressed in simulated operating conditions; injecting 18 different 155 Mbit/s patterns into the parallel paths to pinpoint the effect of reflections, cable losses, and connector crosstalk. A typical result of these tests for a cable 9 m long, terminated at the receiving end, is shown in this slide.

Slide #45

Simulated 155 Mbit/s Eye Patterns



Despite the fact that single ended signals at the receiver appear to be affected by a significant amount of noise, the differential responses are good thanks to the cancellation of common mode noise, as shown by the eye-diagrams in the slide.

Slide #46

Final Results

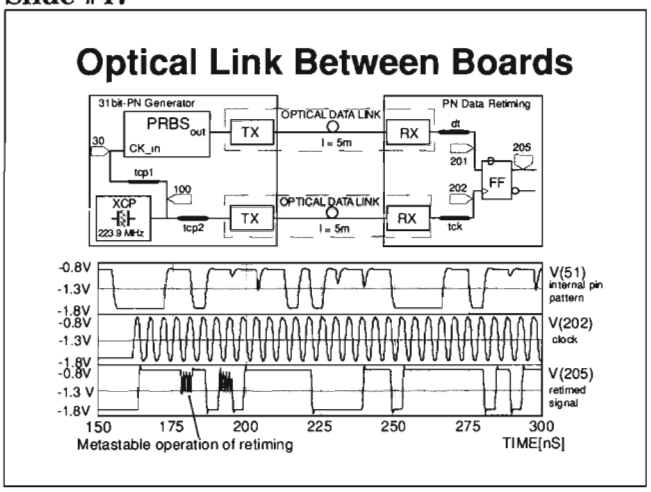
Concurrent design needed
(interconnects have a great impact on architectures)

Total throughput of 30 Gb/s per board feasible
(up to 10 m length, electrical solution)

I/O interface power dissipation becomes
the limiting factor

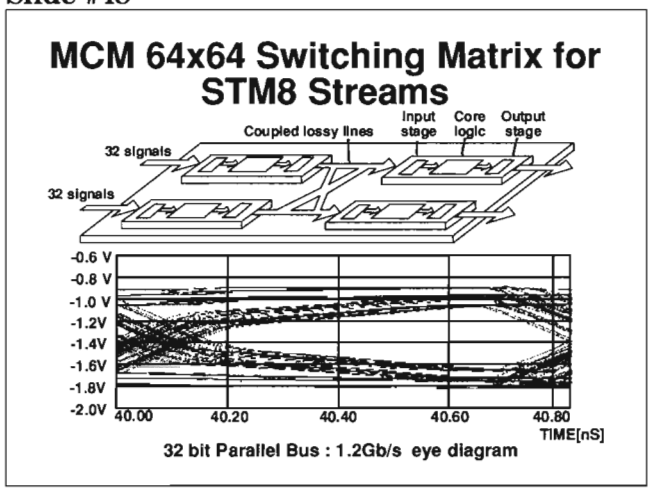
The results of the previous case study demonstrate the feasibility of an electrical backplane interconnect at a data rate of 155 Mbit/s per channel. The use of high-density connectors allows a global I/O throughput of about 30 Gbit/s per board, assuming that about 500 pins are used for high speed ATM streams (each balanced channel requires 2.5 pins). The major issue becomes power dissipation of I/O interfaces. The need to address interconnect problems as early as possible in the design phases (concurrent design) has again been emphasised in this case study.

Slide #47



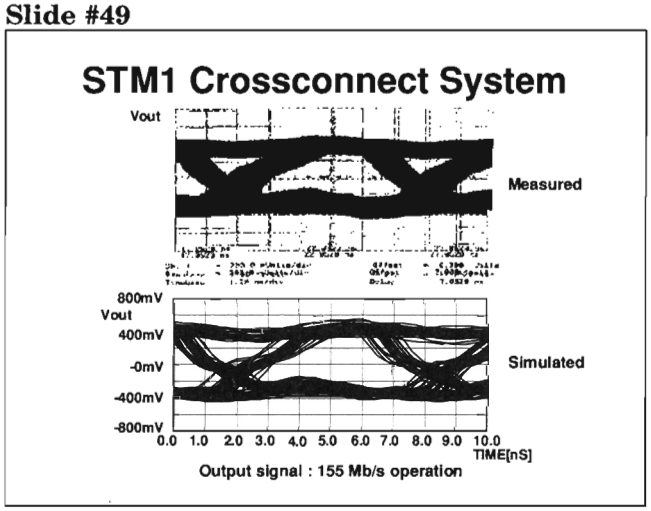
Optical interconnects are playing a major role in telecom apparatus because they may overcome some of the bottlenecks of their electrical counterparts. This slide shows a digital subsystem including a 223.9 MHz quartz crystal oscillator, a Pseudo Random Binary Sequence (PRBS) generator board, and a retiming board connected at backplane level by two optical data-links carrying clock and data streams, respectively. The optical modules include an LED driver, a 1st-window LED (HP BR1414), a PIN-preamplifier module (HP BR2416), and an ECL post-amplifier. The optical cables are 50/125 um, 5-meter long multimode fibers. The entire sub-system has been modelled and simulated at the electrical, timing, logical, and optical levels to check its overall performance. The faults due to timing problems, like metastable states, can be also easily pinpointed. About 30 seconds are required on an HP 750 workstation to carry out the whole simulation (1,300 elements x 6,000 timepoints).

Slide #48



This slide shows a Telecom application regarding a 64x64 crosspoint switch operating at 1.2 Gbit/s implemented on MCM-D technology. All lines are modelled behaviourally as lossy interconnections taking into account skin effect and DC losses. Simultaneous switching and non-ideal power distribution are also modelled. Parallel buses are treated as lossy coupled lines, and crosstalk due to modal velocity differences is also taken into account. All models are obtained through TDR/TDT measurements of actual devices, using a deembedding procedure to discard the effects of test-fixtures and packages. Each bare-die holds 32 simultaneous switching drivers and 32 receivers. Core-chip functions are also implemented as VCVS generators. The overall model complexity is about 5,000 elements.

Slide #49

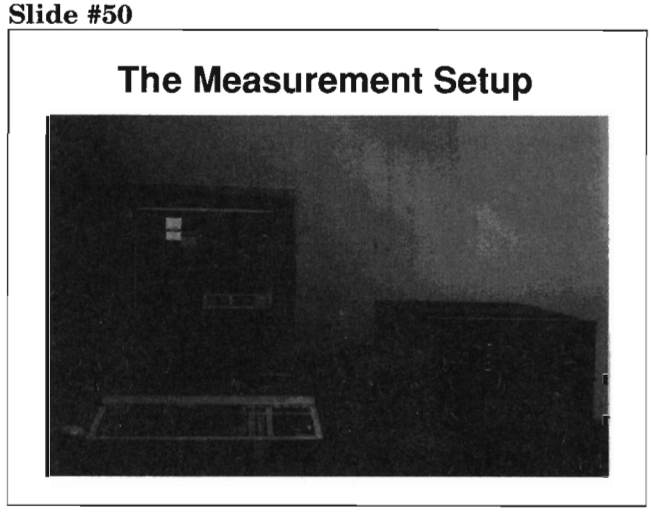


For telecom system validation, the BTM methodology allows the simulation of very complex systems with various input patterns. This slide shows the 155 Mbits simulated eye-diagram at the output of a digital crossconnect compared to the actual measurement.

The crossconnect system is composed of several switching boards, placed in different racks connected together and to STM1 peripheral ports.

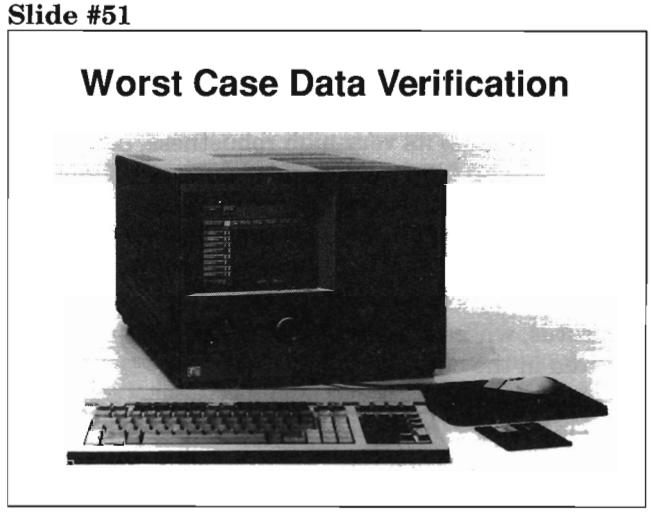
The complete model of the crossconnect counts more than 50,000 electrical/behavioural elements (switching elements, boards, connectors, cables). The 32 simultaneous input sequences are composed of 64 random bits each. All signal degradation effects, including pin bouncing and timing skews of each crossconnect, are taken into account. Simulation time of the entire system for 16,000 time points is about 1 hour on an HP 750 workstation.

Slide #50



Shown above is a picture of the measurement setup used in this paper. The setup contains an HP 54120-series high-bandwidth digital oscilloscope, an HP 750 workstation, and the modelling and simulation software by HDT, described on the next several pages.

Slide #51



SPRINT produces a worst case bit sequence from its simulation results that will cause maximum eye-closure of the simulated or measured signal. In the case study an HP80000 Data Generator System, as shown in the above photograph, was loaded with this bit sequence. It was then used in conjunction with an eye-diagram measurement made on an HP54120 oscilloscope to verify the performance of the ATM prototype.

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This stage is vital to verify real-world performance during prototype debug. The combination of precision measurement equipment and simulation software used here makes the complete debug process extremely effective.

Slide #52

SPRINT: The New Simulation Engine

Digital signal processing ⟨ very high speed

No convergence problems

Supports RLC, TLM, and BTM models

High complexity net simulations (limited only by available workstation RAM)

SPRINT is the simulator used in all the examples presented in this paper. Its main characteristics are 1) its simulation speed, which can be orders of magnitude greater than conventional time-domain simulators and 2) its very high robustness, because convergence problems are avoided even in the most complex situations. Its speed, due to proprietary DSP (Digital Signal Processing) algorithms, plays a fundamental role in model validation and in the simulation of complex systems, typical of telecom apparatus, where a high level of interactivity is required in the optimisation process. The SPICE-like system description can include transfer functions taking into account logic, timing, and behavioural (time-domain, S-plane, Z-plane) issues, as well as non-linear effects. In addition, the simulation can be carried out simultaneously at all levels. Behavioural time models, as well as other modelling techniques, like TLM (Transmission Line Modelling), effectively take into account propagation effects, along with conventional RLC equivalent circuits, and are fully supported by the SPRINT simulation engine.

Slide #53

The Graphical Environment: SIGHTS

PWL fitting supported

Eye-diagrams

Worst case eye-diagrams

Worst case binary pattern generator

Signal template specification

SPRINT's output waveforms, as well as those coming directly from measurements, can be further processed within the graphic environment, SIGHTS, that also support a set of signal quality evaluation tools including:

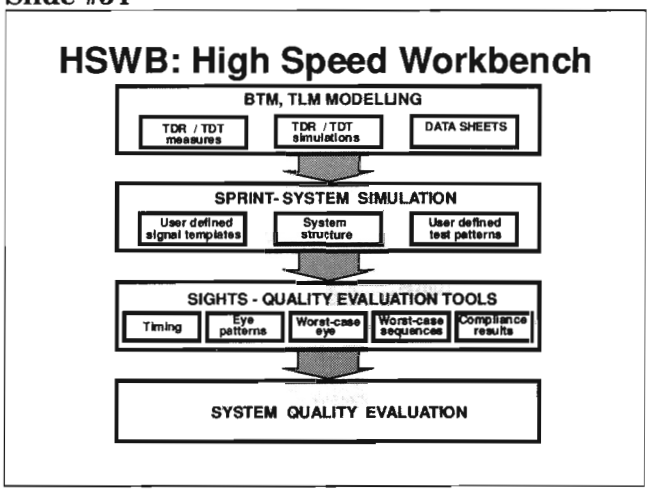
- Eye-diagram display of signals for the evaluation of quality parameters including eye opening, noise margin, and time jitter.

- Calculation of worst case eye opening starting from a simulated or measured single transition. The digital bandwidth of components and systems can be quickly evaluated in this way.

- Worst case binary pattern generation. This pattern, causing the maximum eye closure at a given bit-rate, is very useful for generating test vectors to stimulate both simulated systems and actual prototypes. In this last case, the vectors can be loaded into a high-speed pulse pattern generators, such as the HP 80000A data generator system, for real-time verification.

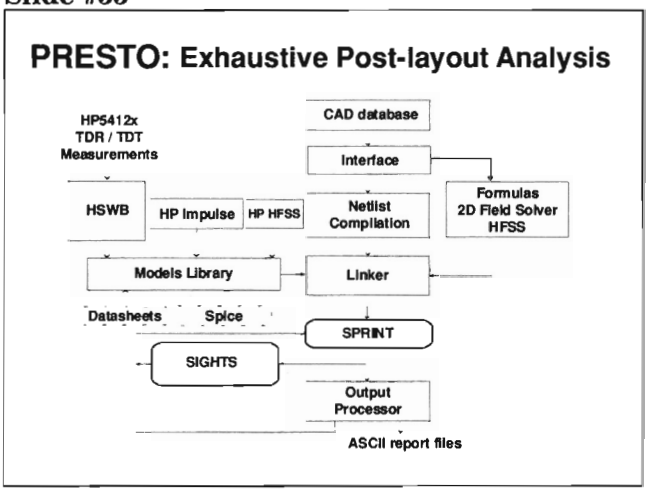
- The signal template specification is a very effective technique used to carry out compliance testing at system's standard interfaces or to check signal quality within the system itself. Moreover, it is very useful to evaluate a system's global quality when a graphic display of a waveform is impractical, due to huge number of test points as usually happens in exhaustive post-layout simulation of PCBs or MCMs.

Slide #54



The previously mentioned modelling, simulation, and quality checking tools are fully integrated in the HSWB (High Speed WorkBench) environment, that links wideband time-domain instruments to SPRINT & SIGHTS, as shown in the slide. The instruments are connected to the workstation via an HP-IB or RS232 serial interface and the acquired waveforms can be stored in SIGHTS format for further processing. Using HSWB, the user can quickly extract models from wideband TDR/TDT measurements, carried out on hardware components, including ASIC, packages, PCB traces, connectors, backplanes, cables, and even optical components. TDR/TDT component characterisations can also be performed in a simulative way using tools like SPICE or HP IMPULSE, if working at transistor level, or for ultimate accuracy from 3D field solvers like HP's HFSS, when technological and geometrical parameters are available.

Slide #55



PRESTO is the environment linking the hardware models obtained from TDR/TDT measurements to CAD databases to perform automatic pre- and post-layout analysis of entire PCB, MCM or Hybrid designs. Topological and geometrical information extracted from a CAD database is automatically converted into a SPRINT netlist, including electrical/behavioural models of interconnects and active devices. The experimental way is the most accurate method to extract models, but they can also be obtained from simulated TDR/TDT tests using other electrical simulators, such as the HP Impulse product, or 3-D field simulators, like HP's HFSS.

Exploiting SPRINT's features, it is possible to analyse the whole system within the same simulation run including transmission, crosstalk, and switching noise effects, simultaneously. This is the only way to get reliable results, because all drivers are loaded with their actual load. Input to output timing delays and even logic behaviour can be included in the models, so that simulation can also treat these issues with signal integrity in mind. The user can perform a complete compliance analysis of all signals with respect to user defined signal templates getting a global report that contains the list of nets with their violation errors. The effects of non-ideal power and ground planes, as well as EMI/EMC evaluation, will be available in the near future.

Slide #56

PREST0: Demo Board Test Results

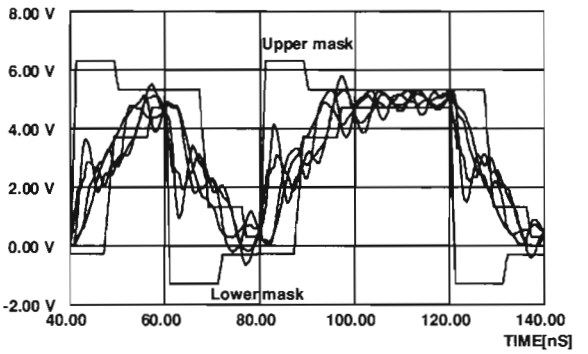
Number of Nets: 488
Number of Components: 228
Number of Elements: 13492
Number of Nodes: 6255
Extraction Time: 2 min*
Compilation Time: 1.5 min*
Simulation Time: 1.5 min*
Total Time: 6 min*

* On a HP750 workstation

Shown are the main results related to multilayer PCB post-layout analysis. This board contains about 200 components and 500 nets. The total analysis time including extraction, netlist compilation, and SPRINT simulation is about 6 minutes on an HP 750 workstation. Thanks to this speed, it is possible to dramatically reduce design and redesign cycle times and enhance product quality.

Slide #57

Exhaustive Compliance Analysis



Shown is an example of automatic compliance analysis of signals performed on the demo board previously described. The waveforms of a critical net and the user-defined signal templates are displayed to point out violation errors. An automatic violation error evaluation is carried out for each net and then stored in a report file. A global violation error is also detected to get a figure that represents the quality level of the whole board.

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Performance & Quality: the Key of Success

Pre-layout analysis

Design rule setting
Performance optimization

Post-layout exhaustive checks

Reliability enhancement
EMI/EMC evaluation
Faster prototyping and validation

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Recommended Resources

- Equipment and accessories
  - HP 54120-series oscilloscope
  - HP 80000A data generator system
  - HDT high-speed workbench including: SPRINT, SIGHTS, and PRESTO

Focusing on performance and quality issues is the way to be competitive in the Telecom market. System manufacturers and service providers will be more and more deeply involved in these two major issues so that new design and test tools are strongly required to face them. This paper has shown some applications of an integrated measurement and simulation environment that offers unique help in design and validation of telecom apparatus. Tight integration among wideband time domain instruments, behavioural modelling procedures and a powerful simulation engine are the key features of this environment. A great number of actual applications, including design and validation of broad-band telecom switches, have demonstrated the effectiveness of this approach and its benefits.

Experience suggests the systematic use of this kind of tool to perform pre-layout analysis to set design rules to follow during the physical implementation. In this phase, it is also possible to optimise system performance to solve physical layer bottlenecks. Exhaustive post-layout checks, including signal compliance analysis and EMC/EMI evaluation, performed on routed boards and possibly extended to the entire apparatus, is the best way to verify and enhance the quality of hardware before its implementation and can greatly help both prototype debug and system validation.

References:

[1] "TDR Techniques for Differential Systems", HP AN 62-2
[2] SPRINT&SIGHTS APPLICATION HANDBOOK, HDT
[3] "Passive Components Modelling based on Reflectometer Measurements", HDT AN-01
[4] "Modelling of Active Components", HDT AN-02
[5] "Design and Validation of High Speed Optical Data-Links", HDT AN-13