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Glitches, Intermittents and Noise . . . Building in Reliability

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Abstract

What are the major causes of intermittent failure in digital designs? What is the origin of these causes? What can be done to minimize these failures? This paper discusses these issues and more including tips on building in reliability through noise budgeting. Case studies are used for illustration and examples.

Authors

Greg Doyle

Current Activities:
Greg Doyle is vice president of Integrity Engineering. He is currently active in the development of system level design and screening tools to ensure signal integrity and reliability. Greg has also given numerous workshops on high speed design.

Author Background:
Greg graduated from Michigan Technological University. He worked five years with Control Data in mainframe computer development before founding Integrity Engineering.

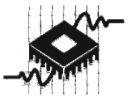
Bernard Sheehan

Current Activities:
Bernard Sheehan is the chief technical consultant at Integrity and has contributed proprietary methods for Boundary Element analysis, crosstalk simulation, and transmission line modeling including frequency dependent losses.

Author Background:
Bernard graduated from Carleton College, MN, and the University of MN. He also worked five years with Control Data in mainframe computer development before founding Integrity Engineering.

Slide #1

Glitches, Intermittents and Noise ... Building in Reliability



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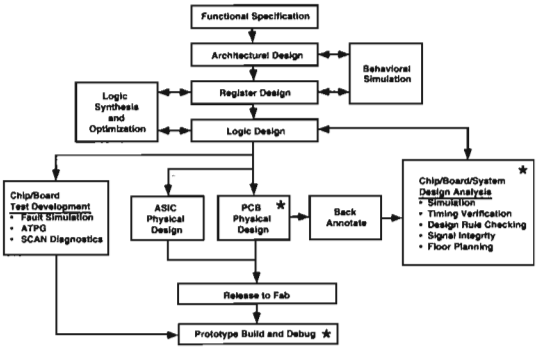
Slide #3

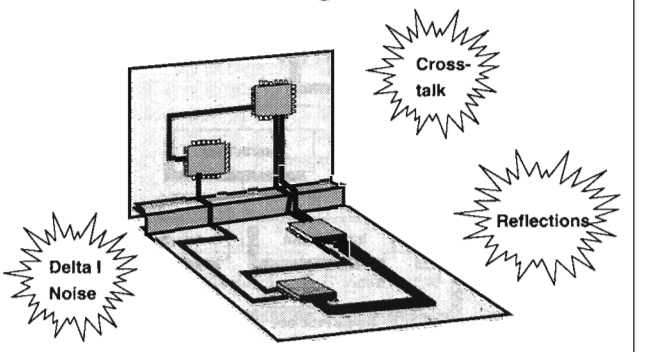
Simplified HS Digital Design Process



The areas of the Simplified Design Process this talk deals with are highlighted as shown here with asterisks.

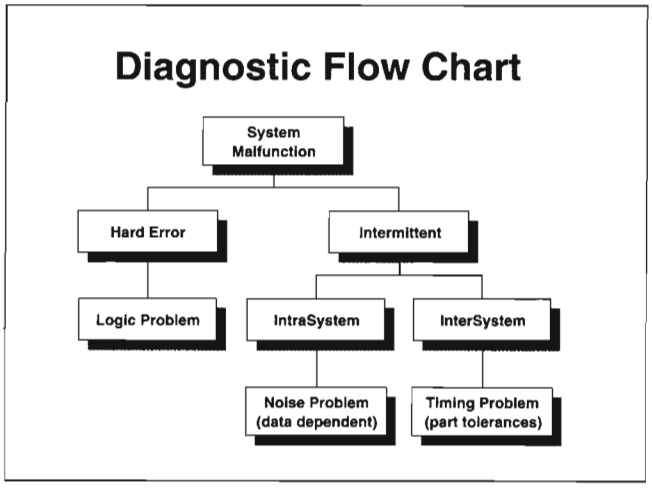
Slide #4

What is Causing the Glitch?



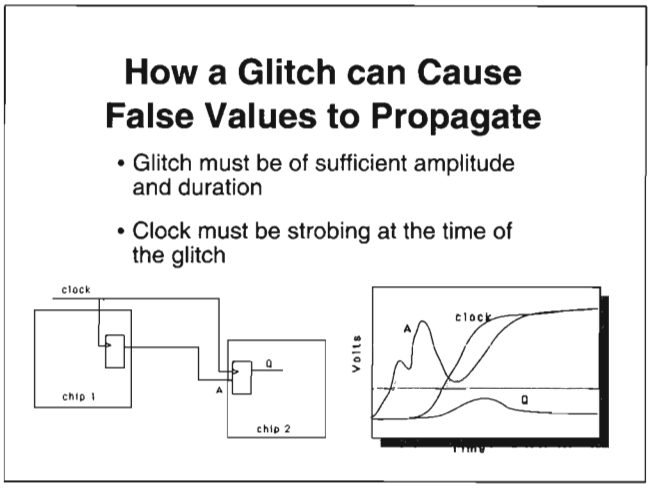
If your system has intermittents, how do you go about discovering the source of the problem? Where is the glitch coming from? How can you design to avoid glitches? Obviously, there is no simple, universal way to answer these questions. But knowing the characteristics of different noise sources and how to isolate and quantify them can assist you in "Zooming in" on the problem and eliminating its cause.

Slide #5



Troubleshooting digital system problems is very much like detective work. Each case is unique and draws on the reasoning powers of the engineer solving the problem. This slide suggests a high level flow chart for isolating the cause of digital errors. A logical error is a hard error that will show up consistently in all systems. Timing errors may be present in some units and absent in others, depending on the variations of parts in each unit. Noise problems are intermittent within the same unit, depending on data patterns and activity in other areas of the circuit.

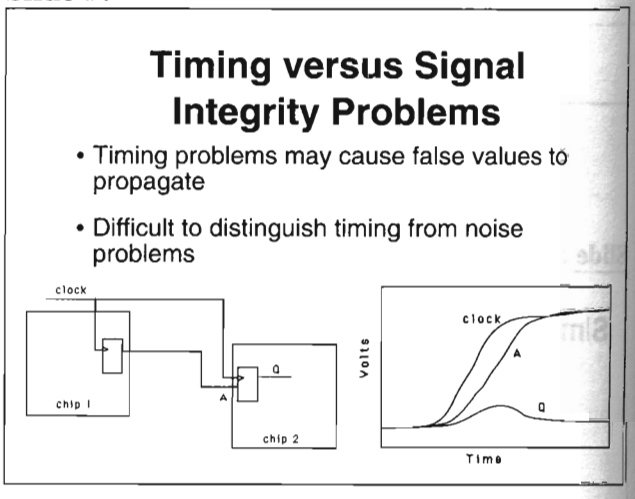
Slide #6



Normally, each stage of logic filters out the noise at its input, producing a clean output pulse for the next stage. This makes for very robust performance.

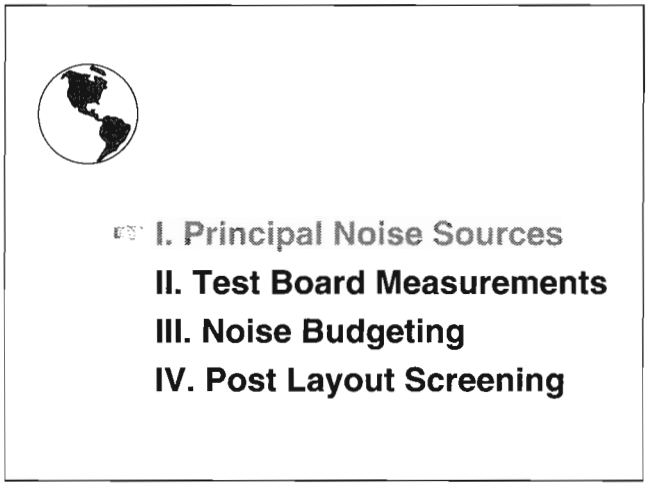
However, under certain conditions, the wrong value can be clocked into a flip flop. This will be the case, for example, if a large glitch occurs at about the same time as the clock strobe. This glitch must not only occur at the right time, but also be of sufficient amplitude and duration to cause the flip flop to interpret the input as a low, rather than of a high.

Slide #7

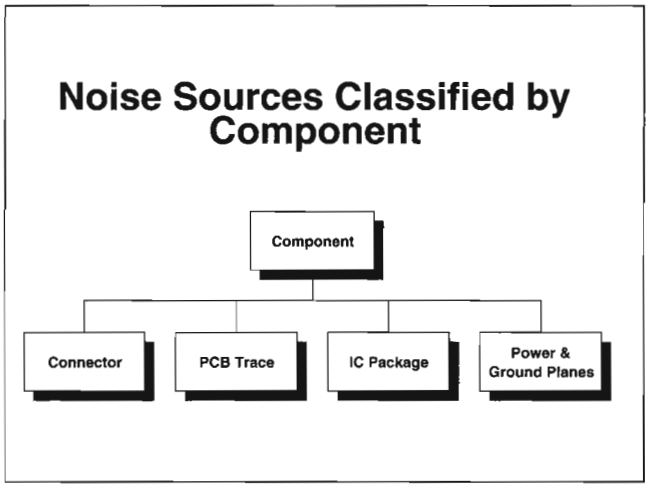


Unfortunately, timing and noise problems often have very similar symptoms. Both can cause the wrong logical values to propagate. One has to inspect the signals at the input of the flip-flop to see whether the signal is simply delayed or badly distorted. Since noise may cause extra delay, a path with marginal timing might fail when extra delay from signal noise is added. In this situation, the failure is due to a mixture of timing and noise problems.

Slide #8

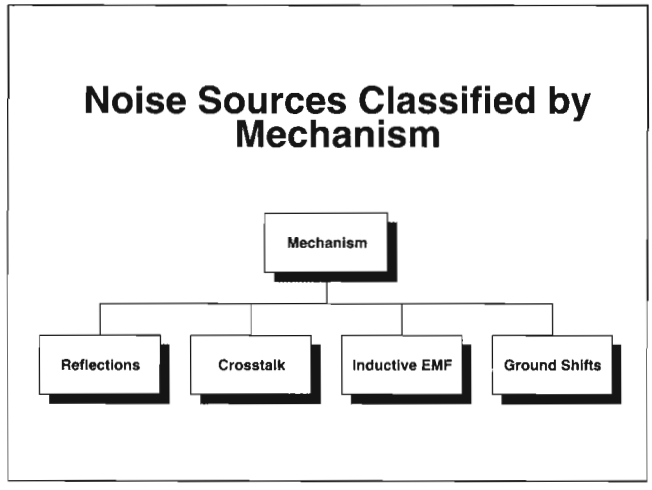


Slide #9



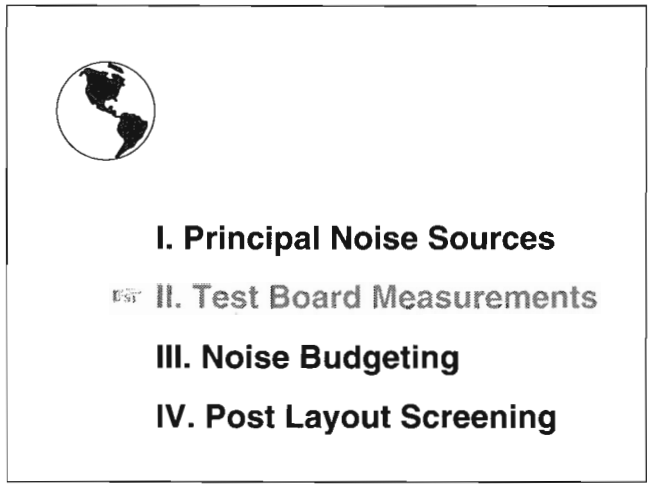
One useful approach to track down the source of glitches and intermittents is to consider the noise generating abilities of each component in your system. The same component may be responsible for several forms of electrical noise. For example, an IC package may cause delta I noise, crosstalk, and reflections. Or PCB traces may cause crosstalk, IR drop, and stub reflections. Sometimes a glitch may be produced by a single component (like a connector with inadequate thru-grounds); other times it may be the sum of noise contributions from several components.

Slide #10



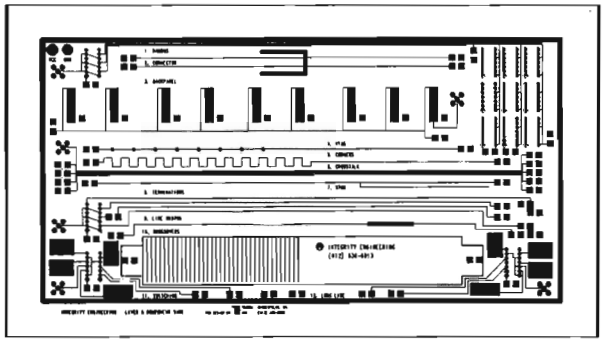
It is also useful to recognize the different mechanisms that generate noise. As already noted, the same mechanism may be operative in several components. Crosstalk, for example, may occur along the entire signal path—it may occur in the driver package, along the printed circuit traces, in any connectors along the path, and in the receiver package.

Slide #11



Slide #12

Signal Integrity Test Board



To illustrate various glitch producing mechanisms, a signal integrity test board with twelve "experiments" was designed. Measurements from this test board will be used to illustrate the noise effects being discussed in this paper.

The board is a 12" x 6" FR4 printed circuit board. The layup consists of a surface signal layer, a ground plane, a power plane, and a solder layer on the back. The default line width, which was designed using IEI's CALIF software, was 11 mils; this resulted in an impedance very close to 50 ohms. Active components for driving and loading traces consist of 74F04 or 74HC04 hex inverters.

Slide #13

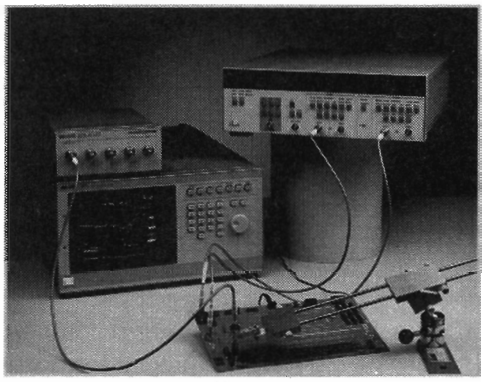
Measurement Setup

- **HP 54120A Oscilloscope**
- **HP 54124A Test Set**
- **HP 8130A Pulse Generator**
- **HP 54720A (Single Shot Glitches, Intermittents)**
- **ICM TDR Probe Assembly**

An HP 54120A oscilloscope was used for all of the measurements. Its TDR (Time Domain Reflectometry) capability makes it ideal for investigating reflections and impedance discontinuity effects. For driving lines, an HP 8130A Pulse Generator was used. Its programmable period, pulse width, amplitude, and rise/fall time are valuable for looking at how crosstalk, for example, depends upon the pulse characteristics. HP 54006A Resistive Divider Probes were used to give wide bandwith and low capacitive loading.

Slide #14

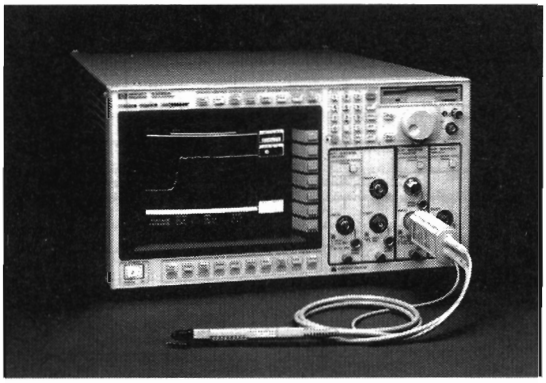
Measurement Setup (Cont.)



This is a photo of the HP 54120A TDR Oscilloscope and the HP 8130A Pulse Generator – products used in this talk.

Slide #15

Measurement Setup (Cont'd)

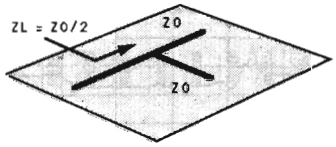


This is a photo of the HP 54720A. Because of its fast digitizing rate (2 Gsa/s w/4 channels, 4 Gsa/s w/2 channels), it is an ideal tool for troubleshooting single shot glitches and intermittents. This particular aspect of troubleshooting will not be covered in this paper.

Slide #16

Reflections

$$\rho = \frac{ZL - Z0}{ZL + Z0} = -\frac{1}{3}$$

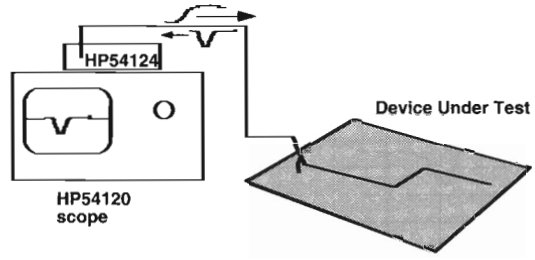


- Routing stubs can produce significant reflections

One key source of glitches are reflections. Routing stubs, for example, can cause negative reflections or glitches equal to 33% of the input signal swing. This noise source alone, can take up most of a logic family's noise budget. This is why high speed designs generally use daisy-chain routing or point-to-point routing, which avoids stubs.

Slide #17

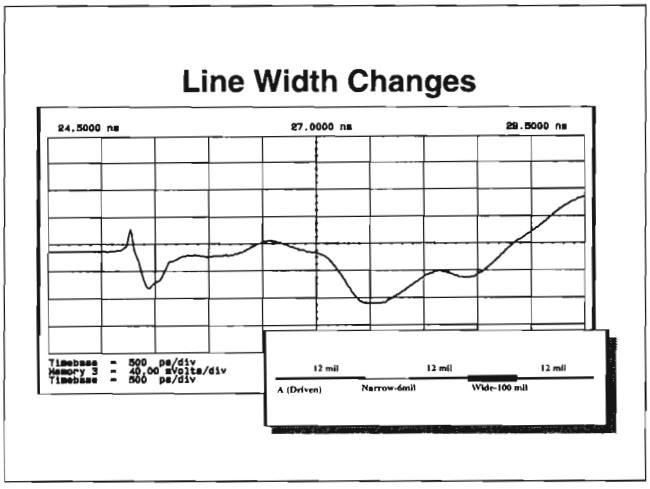
Time Domain Reflectometry



- TDR sends fast risetime pulse down line.
- It displays any reflections coming back.

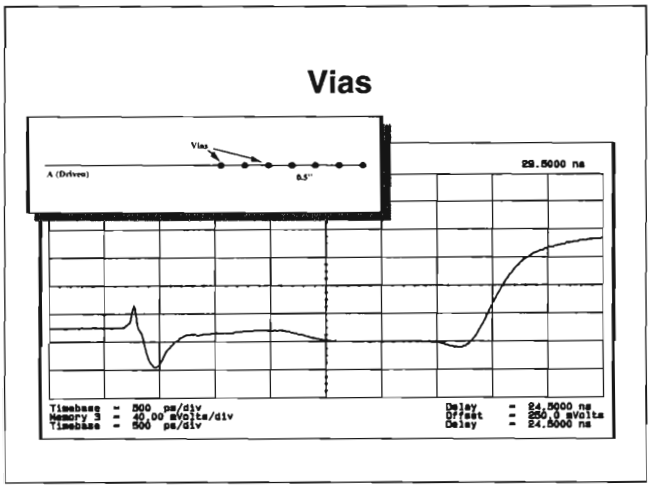
Time Domain Reflectometry (TDR) is a powerful technique for characterizing the impedance control and reflection generating properties of components and interconnects. A TDR test injects a step voltage with a very short risetime down a cable into the device under test. It then observes reflections returning from the circuit. The temporal position of reflections can be related directly to the physical position of the glitch source.

Slide #18



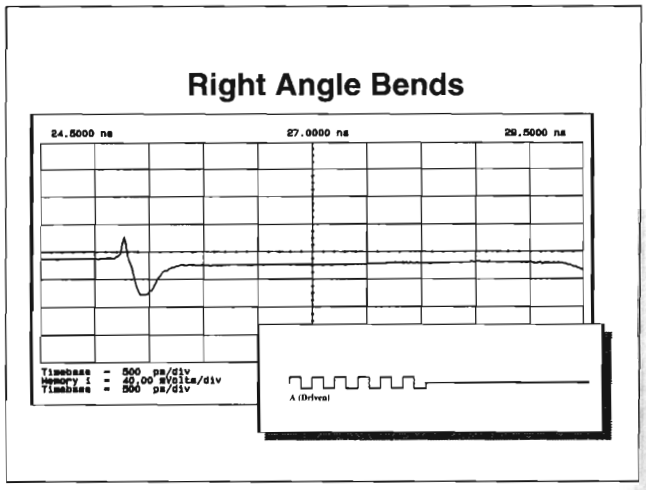
This is TDR measurement of a printed circuit board trace with a width of 12 mils except for a region where it narrows down to 6 mils and another region where it widens out to 100 mils. We see the positive reflection from the higher impedance section of narrower width (65.8 ohm) and the negative reflection from the low impedance section of a wider line (19.8 ohm). The narrow region we call "inductive" and the wide section "capacitive."

Slide #19



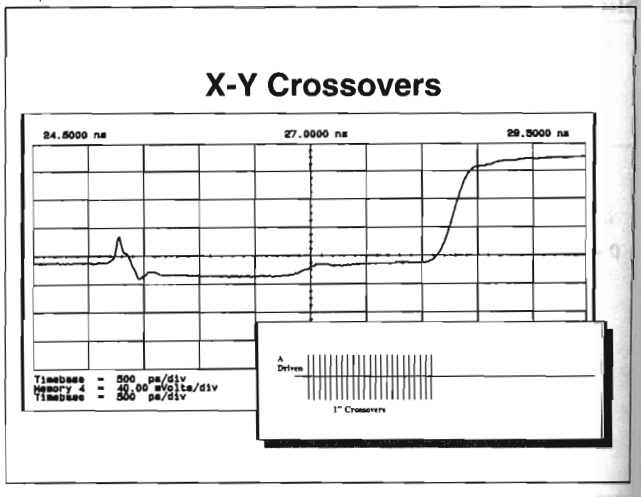
This slide shows the reflections from a line which has through-the-board vias every half inch in its second half. The presence of the vias dropped the line impedance from 50.6 ohms to 43.1 ohms.

Slide #20



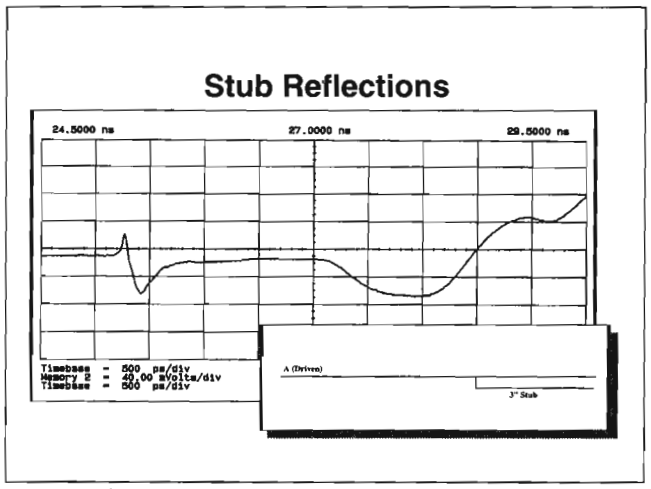
This slide shows the TDR plot of a line the first half of which has corners every 1/4" in its first half, and is simply straight in its second half. The corners have only a slight effect on impedance, dropping it from 50.6 ohms to 48.2 ohms.

Slide #21



This TDR measurement is of the first half of a microstrip line, which passes under a region of perpendicular crossover lines. The crossover traces are 1" long and are at a pitch of 100 mils apart. The presence of the crossovers reduced the impedance from 53.9 ohms to 43.8 ohms.

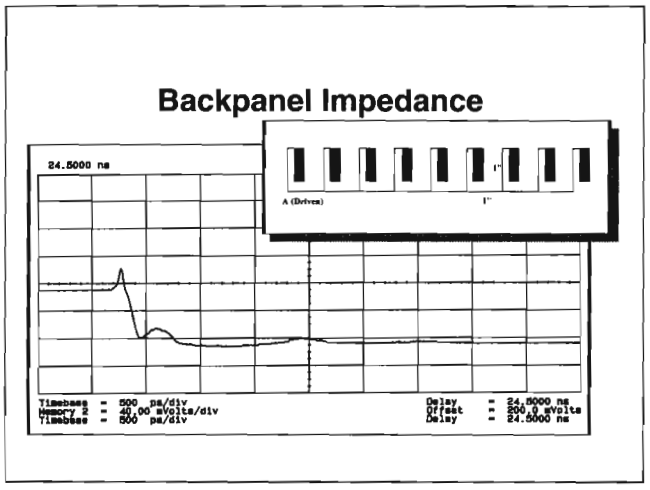
Slide #22



This slide shows the TDR measurement of a 9" long trace with a 3" stub branching from it. The stub causes the impedance to drop from 51.9 ohms to 27.2 ohms. This impedance drop, as already discussed in an earlier slide, is the result of the signal seeing two impedances in parallel.

The detrimental effect of stubs on signal integrity is one of the reasons daisy-chain routing is often used in high-speed designs.

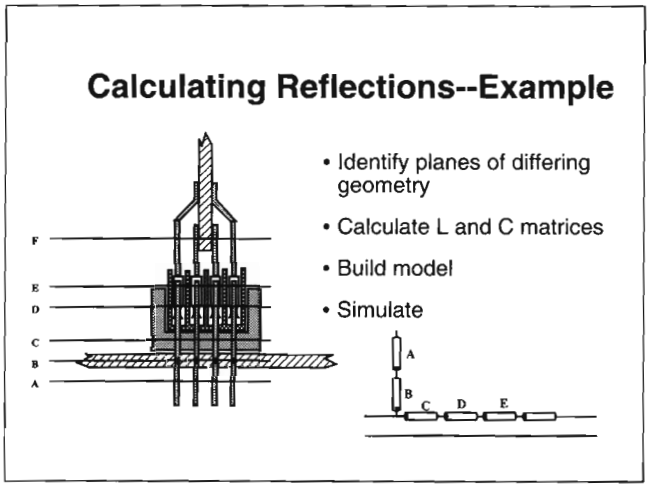
Slide #23



Electrically, a backpanel trace can be thought of as a transmission line with periodic stubs—the stubs representing the loading effect of the daughter cards.

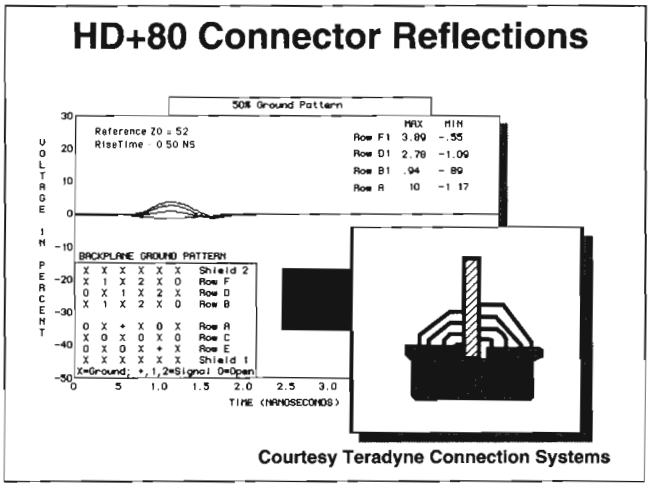
This slide shows the TDR plot of a trace with periodic loads (our idealized backpanel). Just as a single stub pulls down the impedance of a line for a short distance, a periodic arrangement of stubs along the line reduces the line impedance along its entire length. In this instance the impedance was reduced from a nominal 50 ohms to 19.4 ohms.

Slide #24



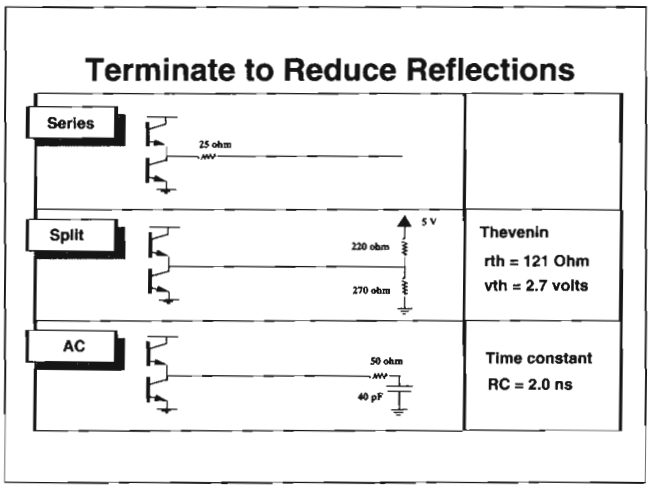
A connector can cause significant reflections (and crosstalk) if it is not designed properly. This slide indicates how the reflective properties of a connector might be calculated. First, planes through the connector where its cross-section changes significantly are identified. Next, using a transmission line parameter calculator like IEI's CALIF, the impedance of a pin at each section is calculated. This impedance, of course, will depend on which pin of the connector are used as ground. Then a SPICE or ALTrA model of the connector may be constructed from a set of different impedance transmission lines corresponding to the different cross-sections through the connector. Finally, a TDR simulation is performed.

Slide #25



The amount of reflection may vary from one row to another in a connector, and will depend on the grounding pattern used with the connector. This slide shows some TDR results versus row for one commercial connector.

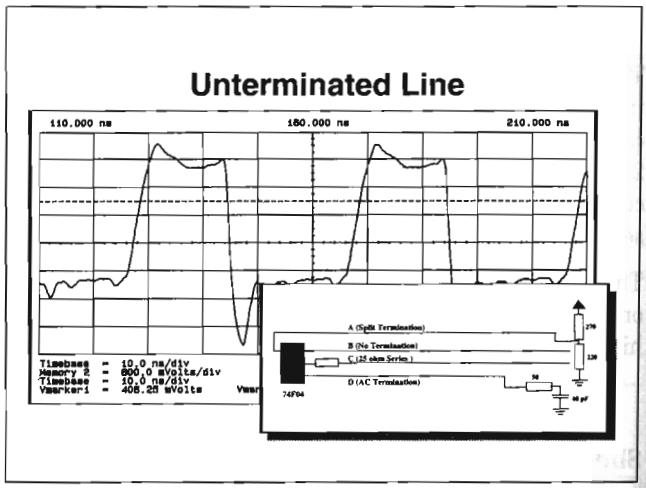
Slide #26



One way to reduce reflections and ringing on a net is by means of some termination scheme. Termination usually involves adding a resistor at one end of the line; there are various ways to do this. This slide illustrates some techniques used with TTL devices.

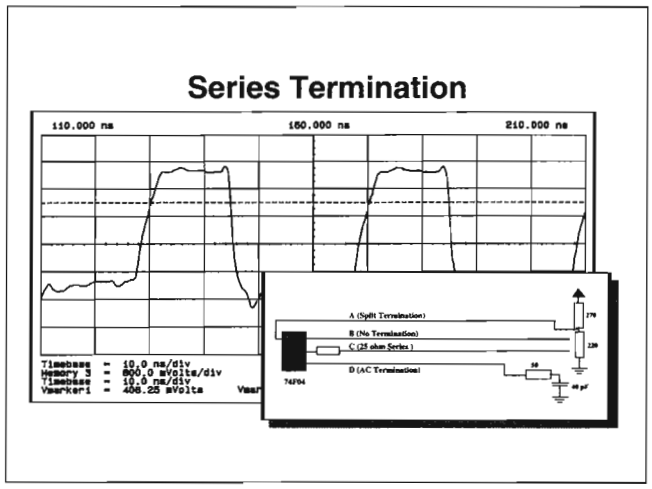
Series termination absorbs reflected energy but does not draw dc current. Split termination biases the line with a certain thevenin voltage and resistance. AC termination absorbs transients but avoids a dc current path that might dissipate too much energy and pull down the output high level. Care must be taken in choosing the right time constant with ac terminations.The importance of these impedance discontinuities may be dependent upon the speed of operation. At relatively slow speeds, these effects may introduce minor response. At higher speeds, the result can be significant.

Slide #27



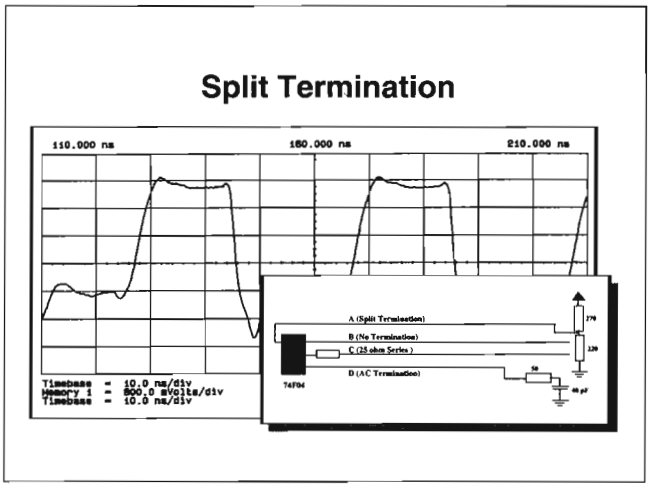
This slide shows a 74F04 output driving a 9" unterminated printed circuit board trace (B). The impedance of the trace is ~50 ohms. Note the overshoot and undershoot.

Slide #28



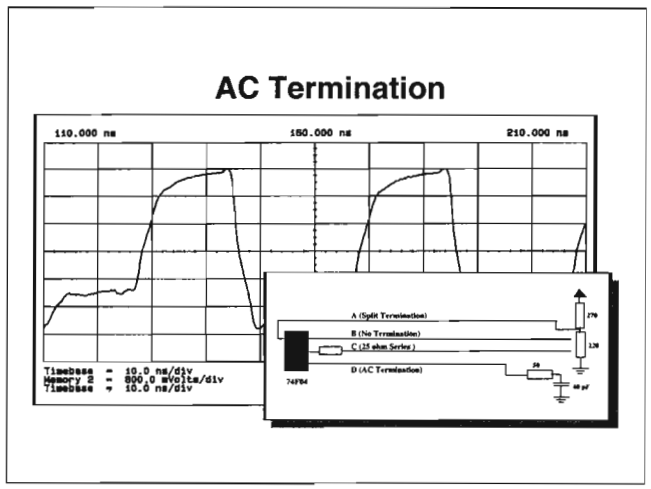
Adding a 25 ohm series resistor at the output (C) reduces both the overshoot and undershoot.

Slide #29



This slide shows a 74F04 output driving a 9" printed circuit board trace terminated with 270/220 ohm resistors (A). Split termination eliminates some overshoot but tends to pull up the output low level.

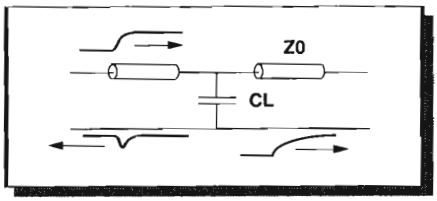
Slide #30



This slide shows a 74F04 output driving a 9" printed circuit board trace terminated with a 50 ohm resistor in parallel with a 40 pF capacitor to ground (D). In this case the AC termination eliminates overshoot and ringing but also noticeably influences the signal edges.

Slide #31

Reflections

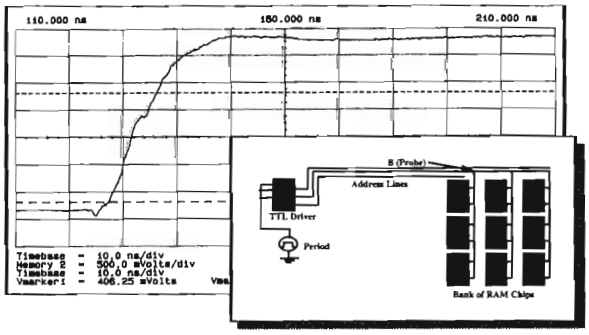


- IC packages can produce significant reflections
- Memory nets can have problems from this

Electrically, an IC package connected to a printed circuit board trace acts like a stub or capacitive load and generates a negative-going reflection. Package reflections become especially significant with large pin grid arrays, which can represent up to 12 pF of capacitance. This is the equivalent capacitance of 4" of 50 ohm transmission line. Designs with nets routing to several large IC packages are prime candidates for glitch problems.

Slide #32

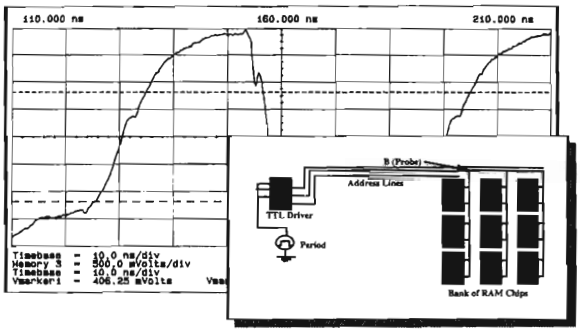
RAM Bank--10 MHz Clock



This example and the next two slides show how the signal looks when it is driving several banks of chips—a configuration that occurs in memory circuits. The signal is measured at point B on the net (at the foot of the first branch). The capacitance of all the branches and IC loads slows the edges (especially the rising edge) significantly. This limits the maximum data rate at which the bus can operate.

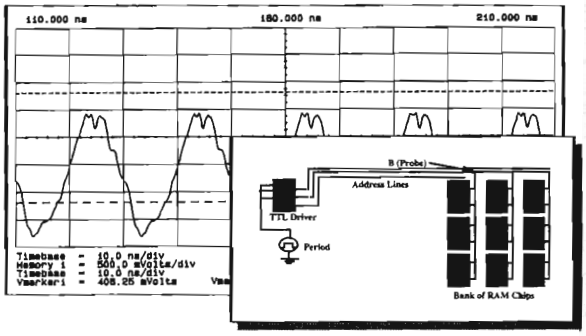
Slide #33

RAM Bank--50 MHz Clock

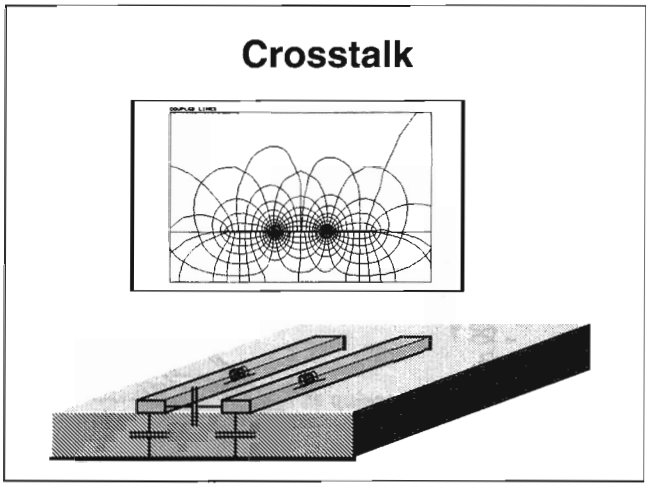


Slide #34

RAM Bank--100 MHz Clock

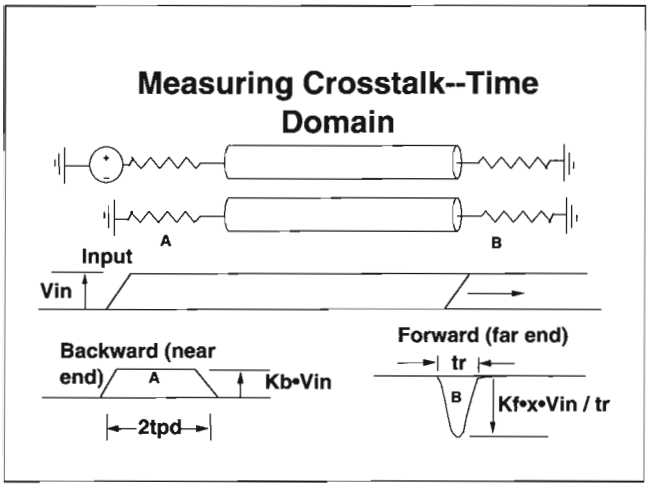


Slide #35



Crosstalk arises from the mutual capacitance and inductance between neighboring conductors. It can be a significant source of noise in densely routed printed circuit boards. Crosstalk may be particularly acute when busses consist of long sets of parallel lines. It can also be significant in connectors with inadequate thru-grounds.

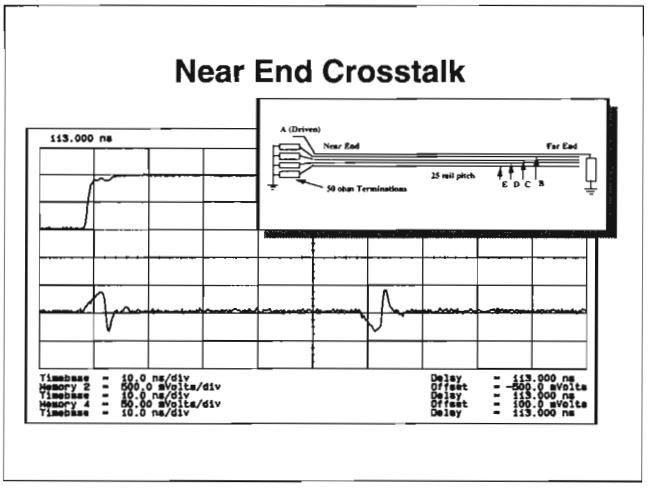
Slide #36



To measure crosstalk in the time domain, we drive one line with an HP 8130A Pulse Generator and observe the waveforms coupled into the near and far ends of neighboring lines with an HP 54120A Oscilloscope.

In addition to measurements, crosstalk can be accurately predicted with CAE tools like IEI's XTALK software.

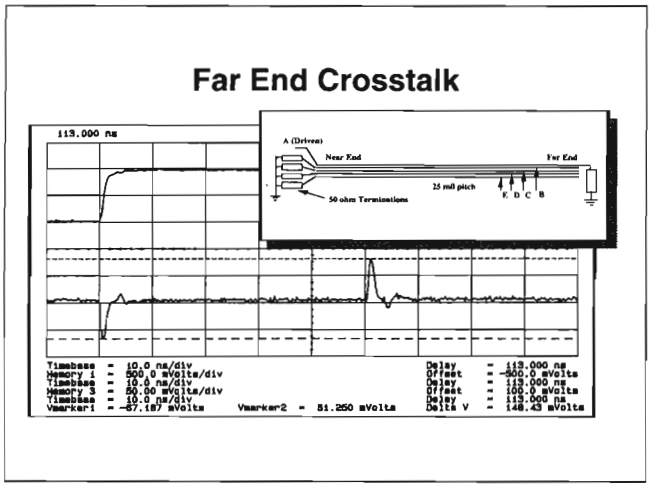
Slide #37



The test board experiment has five parallel 11 mil lines on a 25 mil pitch. The line lengths were about 10 inches. The upper line was driven at one end (point A) and terminated in 50 ohms at the other end. The other four lines are terminated in 50 ohms at their near ends and open at their far ends.

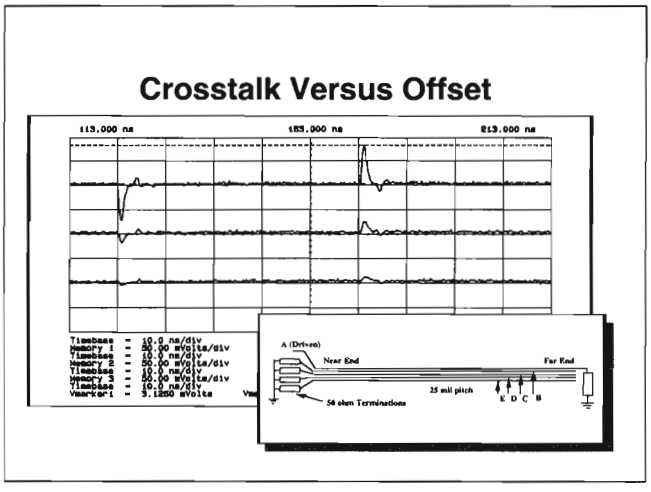
This scope plot shows the waveform at the near end of line B. The waveform includes backwards crosstalk and reflected forward crosstalk.

Slide #38



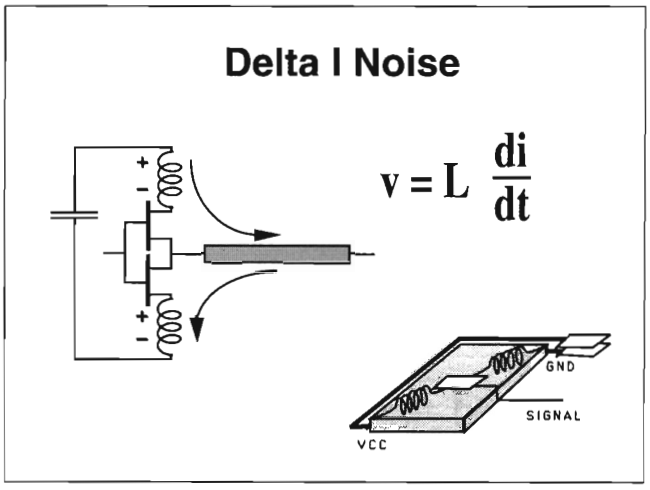
This scope plot shows the crosstalk at the far end of line B. Only forward crosstalk is present; the termination at the near end prevents backward crosstalk from being reflected.

Slide #39



This plot shows that the magnitude of forward crosstalk depends on the distance from the driven line. Starting from the upper waveform, the plot shows far end crosstalk into lines B, C, and D, respectively.

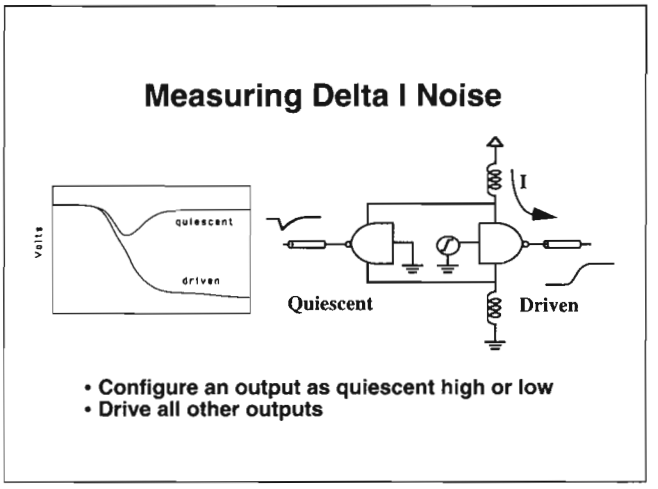
Slide #40



Delta I or simultaneous switching noise can be a significant noise source in digital systems. It arises from the parasitic inductance of the power and ground leads in an IC package. When multiple outputs switch, there is an abrupt change in the current passing through these power and ground leads. The inductive emf due to this sudden change in current causes a voltage spike on the chip's power and ground busses relative to the board power and ground.

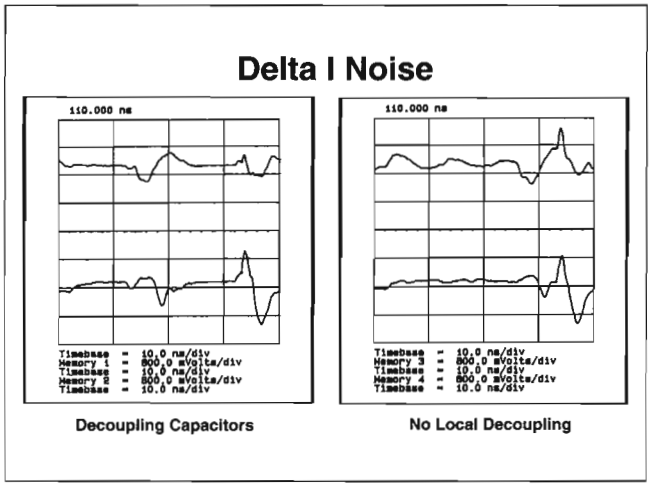
Decoupling capacitors provide local storage for transient current needs. This keeps current loops small (minimizing radiation) and lessens noise on the power and ground planes of the board.

Slide #41



This slide illustrates the technique of viewing the L•di/dt voltage spike on the IC's power rails by looking at the output of a 'quiescent' buffer.

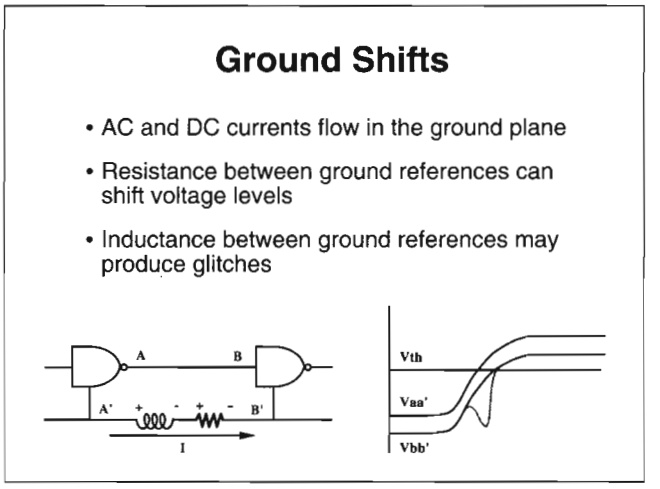
Slide #42



This slide shows the waveforms at the output of quiescent high and low drivers when local decoupling capacitors are present and absent. The device was a 74F04 part; four outputs were driven simultaneously. Of the remaining two outputs, one was held as a static high and the other held as a static low.

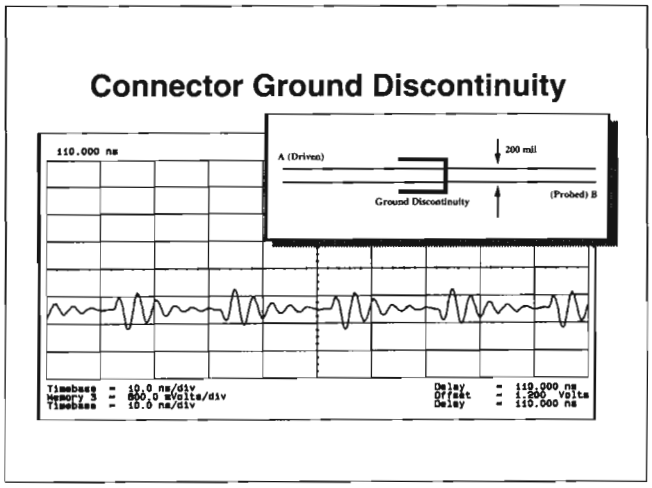
The decoupling capacitors assist in reducing switching noise, but clearly there is still much unbypassed inductance in the IC package.

Slide #43



The power and ground planes (or busses) in a printed circuit board carry both ac and dc return currents. DC currents flowing through the resistance of the ground (power) path shifts the voltage of the signal. Such shifts subtract directly from high or low noise margin. Similarly, AC currents flowing through the parasitic inductance of the ground (power) path will superimpose inductive voltage spikes on a signal. Breaks or interruptions in the ground (power) plane are likely sources of glitches from this mechanism.

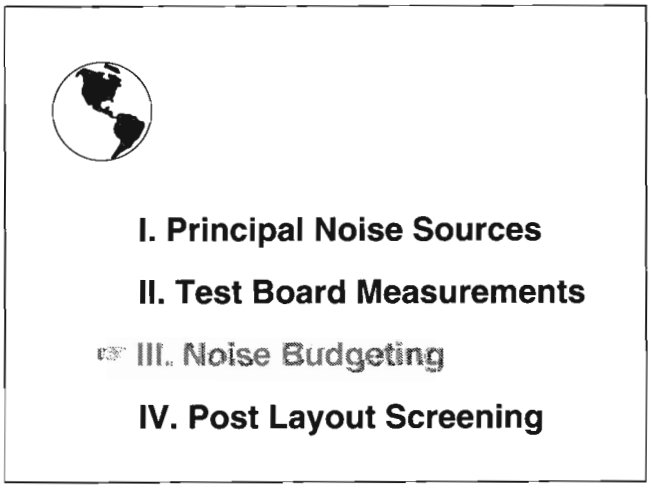
Slide #44



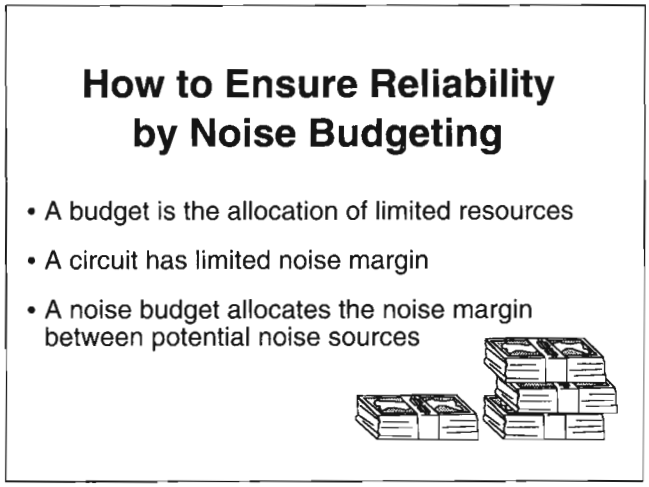
This test board experiment shows how a signal crossing a break or cut in the ground plane sets up a potential difference across the grounds on the two sides of the cut. Moreover, this ground bounce (as it is called) couples into other signals across the same ground discontinuity.

The upper PCB line is driven with a 6V, 1 ns risetime pulse at point A. The scope plot shows the noise coupled into the lower PCB line. The two lines are spaced quite far apart (200 mils), so direct crosstalk between the lines should be negligible. The ringing seen at B is due to the disturbance at the ground discontinuity.

Slide #45



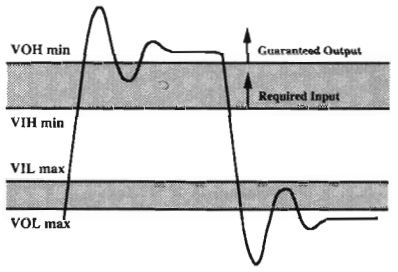
Slide #46



A noise budget is a disciplined way of designing for noise. When you draw up a noise budget, you allocate the available noise margin of your circuits among the various potential noise sources. Then you select/design each component to meet its noise allowance.

Slide #47

The Amount to be Budgeted

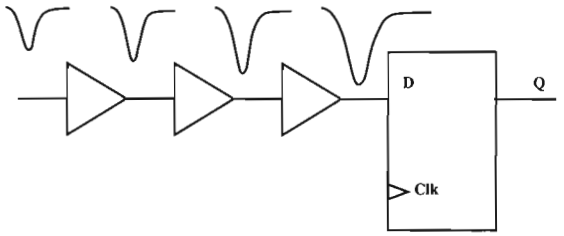


- Noise Margin High = VOH min - VIH min
- Noise Margin Low = VOL max - VIL max

Whether electrical noise causes problems depends on two things: (1) circuit susceptibility to noise and (2) presence and intensity of noise sources in the system. It is common to focus attention on the second item, but the first is equally important. A digital circuit's susceptibility to noise is characterized by the circuit's noise margin. Strictly speaking, there are two noise margins, one for high and one for low logic levels.

Slide #48

Noise Pulse Amplification



A glitch that exceeds noise margin can be amplified by successive stages

If a glitch due to reflections, crosstalk, delta I noise or the combination of these exceeds the noise margin, this pulse can be amplified from stage to stage, eventually reaching an amplitude sufficient to be clocked into a flip-flop or latch.

Slide #49

Noise Margin versus Logic Family

	Voltage Swing	Vth	Noise Margin	REL. Noise Margin
TTL	3.5	1.5	0.4	11%
CMOS	5.0	2.5	0.6	12%
ECL	0.8	-1.3	0.14	17%

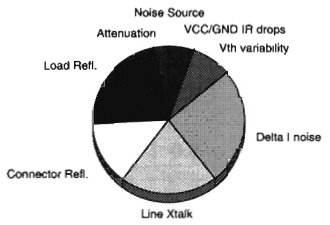
Since the magnitude of noise produced is usually proportional to a logic family's signal amplitude (a 2V signal, for example, will produce twice as much crosstalk as a 1V signal), it is helpful to think in terms of relative noise margin. Relative noise margin equals the noise margin divided by the amplitude of the signal swing. For example, the noise margin of TTL is about 0.4V, compared to 0.14V for ECL. However, TTL signals are also much larger than ECL signals (3.5V swings compared to 0.8V swings). The relative noise margins of the two families are 11% and 17%, respectively.

Slide #50

Sample ECL Noise Budget

Noise Source	Magnitude (mV)
VCC/GND IR drops	30
Vth variability	50
Delta I noise	150
Line Xtalk	120
Connector Refl.	80
Load Refl.	130
Attenuation	20

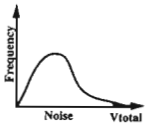
- Noise Margin = 300 mV
- RSS Noise = 253 mV



This slide shows a sample noise budget for an ECL design. If a design were being carried out under such a noise budget, each component would be selected with an eye to its noise allowance. For example, in choosing a connector, one would want to take care to choose a model that keeps reflections less than 80 mV or 10% on the input signal. This may dictate the grounding pattern needed for the connector.

Slide #51

Statistical Addition of Noise



- Electrical noise tends to be random and independent
- This suggests doing root-sum-square addition
- First combine directly noise sources that occur together and in-phase

$$V_{RSS} = \sqrt{V_1^2 + V_2^2 + \ldots + V_n^2}$$

The total noise from many independent sources is not the arithmetic sum of the magnitudes of the individual sources—such a calculation is too pessimistic. The random nature of the noise sources is better taken into account by doing root-sum-square additions. Strictly speaking, such an approach is not rigorous but is useful for guidance in setting up a noise budget.

Slide #52

I. Principal Noise Sources

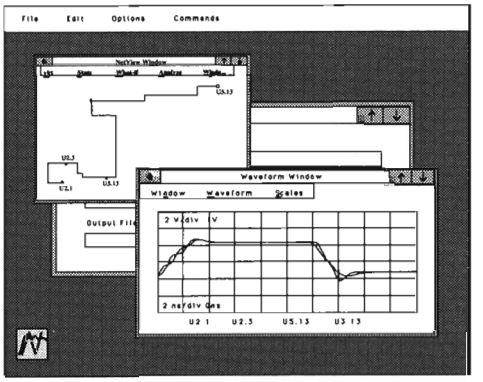
II. Test Board Measurements

III. Noise Budgeting

IV. Post Layout Screening

Slide #53

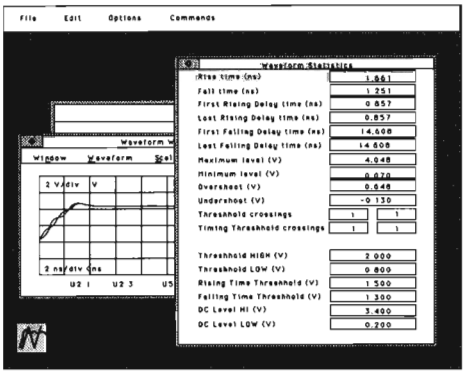
Netview to Screen for Board Noise



To detect potential glitches before committing to a board build, a tool like IEI's Netview in batch mode will simulate every net on a PCB and flag any potential problem nets. These can then be examined individually in Netview's interactive mode, where different possible fixes can be tried until simulation shows good signal integrity.

Slide #54

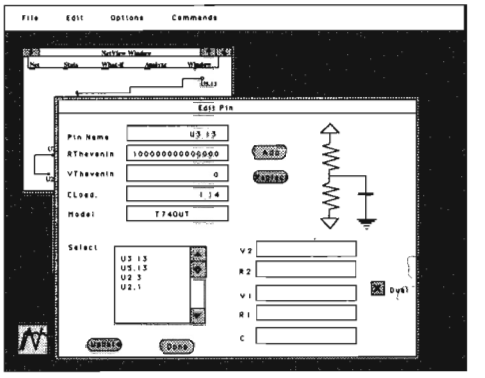
Netview Batch Mode Reporting



Netview will read a routed database and do a transmission line simulation of each net on the board. Waveforms are automatically scanned for excessive overshoot, undershoot, delay, or ringing and nets with potential problems are flagged.

Slide #55

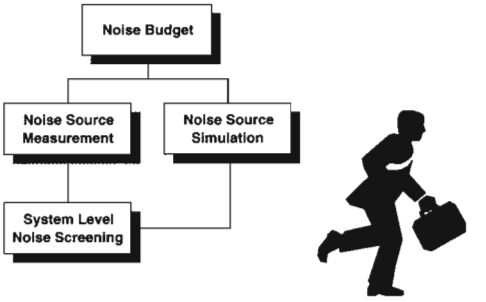
Netview What-if Capability



Netview also has interactive what-if capability, allowing you to try different termination schemes, for example, to fix nets with glitches.

Slide #56

Conclusion: Avoiding Glitches, Intermittents, and Noise



With so many noise generators lurking in your system—delta I noise, crosstalk, reflections, and ground shifts (plus many secondary sources not mentioned)—how can you ensure that your design will be reliable once it is finished? Intermittent noise problems are notoriously difficult to isolate and fix. Clearly a preventative approach is in order. Our opinion is to measure and characterize the glitch generative abilities of each component, and then draw up a noise budget to keep total noise amplitudes within reasonable limits.

Slide #57

Summary--Noise Solutions

- Know the noise margin of your circuits
- Prepare noise budget
- Characterize each component to see if noise is within allotment
- Do final check of design with board level screening software

The best approach to glitches and intermittents is prevention. Know and budget your noise sources.