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Advanced Methods for Noise Cancellation in System Packaging

Henri Merkelo

Ultrahigh Speed Digital Electronics
University of Illinois
1406 W. Green Street
Urbana, IL 61801
Phone: (217) 333-2482
Fax: (217) 333-2736
e-mail: hm@lassi.ece.uiuc.edu

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Abstract

Substantial improvements in signal quality both at component level and system level can be achieved by appropriately balancing the reactive design of digital networks. Cancellation of noise created by components, layout and technologies such as vias, remote grounds and interposer contacts is demonstrated in networks operating from 50 to 200 MHz. This paper discusses the needed cancellation criteria, use of CAE tools and verification of design.

Author

Henri Merkelo

Current Activities:
Henri Merkelo is director of the Ultrahigh Speed Digital Electronics Research Laboratory at the University of Illinois where he is engaged in developing methods for predicting digital signal integrity in systems of high complexity. Both geometric complexity and network complexity are at issue.
Substantial efforts are being expended toward developing simulation techniques capable of including numerous signal degradation effects in complex logical networks. He is involved with the electronics industry in applying these methods to the analysis of advanced and future products.

Author Background:
Dr. Merkelo is on the faculty of the department of Electrical and Computer Engineering of the University of Illinois and is director of the Quantum Electronics Ultrahigh Speed Digital Electronics Research Laboratory which he established. His principal work has been on the engineering and physics of ultrahigh speed electronic and quantum electronic devices and on the study of propagation of short and ultrashort electronic and optical signals, especially as applied to modern packaging technologies. He has chaired technical sessions on the applications of high speed technologies, holds patents on ultrahigh speed electronic and optoelectronic devices and has published numerous papers in his field.
He has directed a number of short courses for the industry on high speed digital electronics and has lectured extensively here and abroad. He is very active in IEEE and in the electronics industry.

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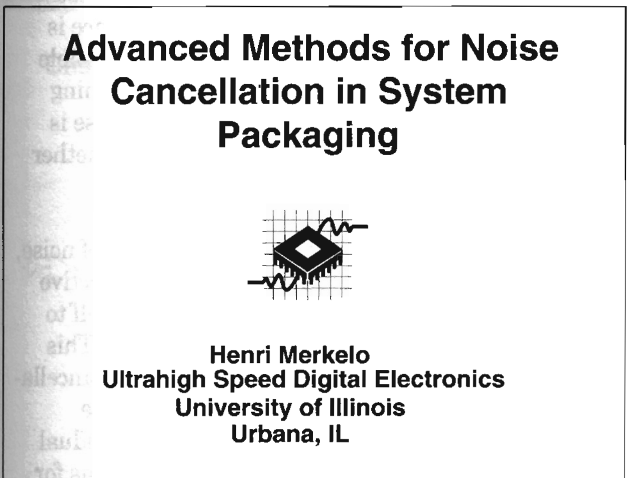

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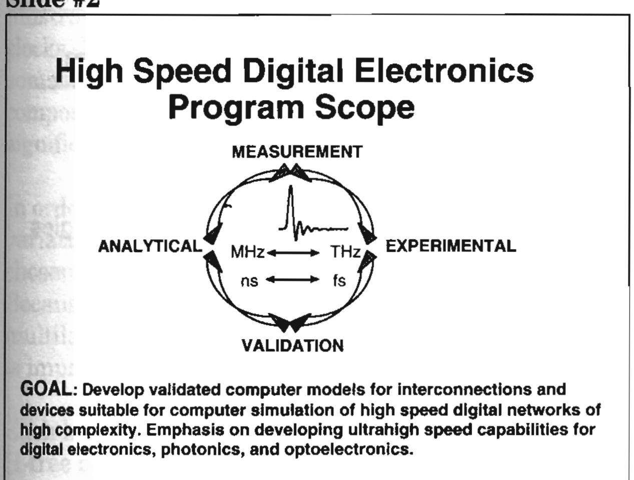

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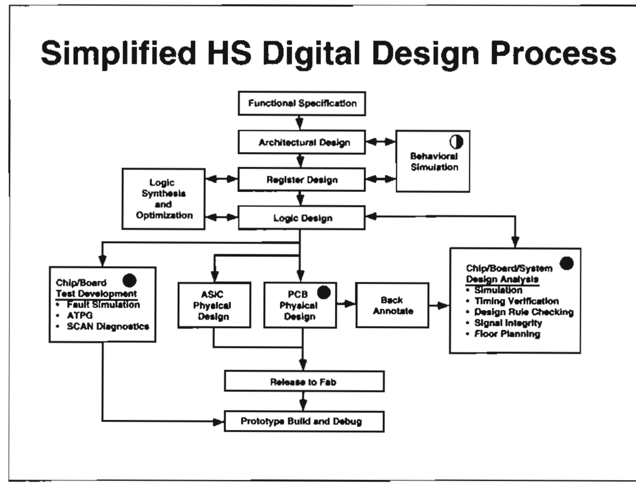

Many systems are designed in such a way that it is difficult to provide signal integrity estimation in the early stages of design because the design methods, the tools, and the technologies are not identified sufficiently early. Whereas it is common to have the IC products chosen at the beginning of the design process, the packaging and interconnection methods and products are often not selected in the early stages of the design. Delaying the decisions on the packaging technologies can result in either an inability of predicting system performance or in an inability of meeting performance expectations. The latter is frequently the case but either alternative has significant market implications. For these reasons and for reasons of being able to achieve the full performance potential of a system concept, reviews and assessments of the packaging technologies need to begin in the early stages of the design process. In particular, packaging design team selection and packaging and interconnection technology choices need to be in concert with IC selection and behavioral simulation.

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Outline

Noise Cancellation in System Packaging

I. System noise: a case study, 50 to 200 MHz
II. Sources of noise; model issues; technologies
III. Principles of noise cancellation
IV. Characterization and compensation
  A. Measurement tools and methods
  B. Advanced computational tools
V. Case study: use of noise cancellation

The position taken for this paper is that the best treatment of noise is its avoidance; if avoidance is not practical, then perhaps cancellation is possible or, at least, partial cancellation. In a self blaming attitude it can be said that digital system noise is designed-in. Therefore, it's only fair to ask whether it can be designed-out.

Fortunately, by studying the characteristics of noise, it can be concluded that noise, especially reflective noise (which causes the most harm) lends itself to cancellation when avoidance is not practical. This paper develops the needed criteria for noise cancellation. The implications of noise cancellation are discussed and demonstrated both on an individual component level as well as on a statistical basis for system level advantage.

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Some Characteristics of Digital Noise

The good news	The bad news
• Noise adds algebraically within the network of one stage of logic or within one clock distribution network.	
• Destructive: ↑ + ↓ = ↓	• Constructive: ↑ + ↑ = ↑
• At each stage of logic noise is filtered out if it is below the noise margins	• Noise signals that exceed noise margins may be amplified by successive stages
• Cancelling effects may leave timing unaffected	• Additive effects can propagate and magnify timing errors

Other than noise of thermal and radiative origins, digital system noise is caused by the arrangement and interconnection of system components and, therefore, has specific characteristics. In particular, within the interconnection network of any one stage of logic or the network of a clock distribution, digital signal noise is algebraic in nature in the sense that given an appropriate time relationship, noise adds or subtracts both to other noise and to digital signals. In this context, a rigorous statistical treatment of noise should follow the principles of the statistics of partial coherence of electromagnetic waves if carried out in the spectral domain. In real time, the treatment would be similar but carried out with waveform distributions, transfer functions and correlation functions expressed in the time domain.

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Within the trends of continually increasing computing speeds and continually increasing system complexities, the task of maintaining digital signal quality is also continually becoming more difficult. Even though the design and test tools for signal management have improved dramatically over the last few years, many deliverable systems nevertheless operate at speeds far below the potential speeds offered by the available component and device technologies and, therefore, do not fully reach their commercial advantage. Methods and tools for managing noise at a component level as well as on a system level are described and illustrated with actual case studies.

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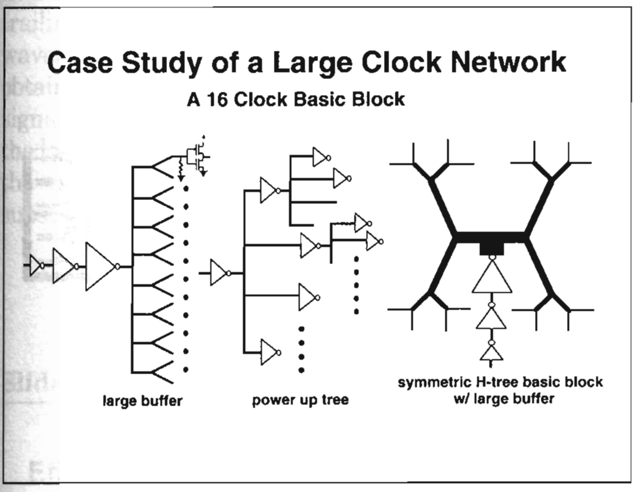

Several aspects of an actual design of a clock distribution network requiring a very large number of clocks, operating at 50, 100, and 200 MHz are used to illustrate and describe several effects. All illustrations are derived from a sub-block of 16 clocks. This number is sufficiently small for gaining some intuitive assessment of the effects of individual components but sufficiently large for observing significant statistical effects.

In order to avoid skew caused by device parameter variations, a large clock buffer driving 16 loads is chosen instead of the so-called power up tree option. Because of the complexity of the boards and multilayer layout of this assembly, a power-up tree is impractical anyway.

Each large buffer is then made to drive a so-called H-tree basic block which is designed to feed sixteen clocks or loads by a succession of transmission line divisions. Each time a transmission line forms a fan-out of two, the nominal impedance is increased by a factor of two. Ideally, in this arrangement, the signal flows toward the load without reflections. The diagram of the basic block is shown with progressively thinner lines suggesting an actual layout of microstrips or striplines.

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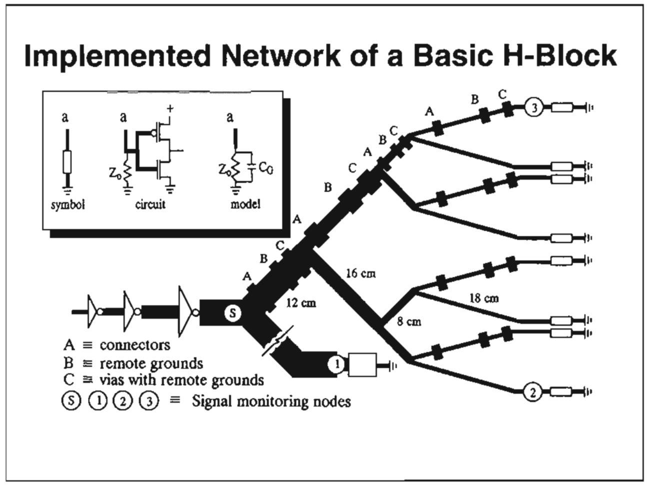

The network is implemented with a combination of several microelectronic packaging technologies which are discussed later in the presentation. As in all systems of high complexity, the implementation of these technologies is imperfect. In this case, signal and ground paths separate for a short distance at the vias, the connectors are not uniformly controlled impedance, the signal and ground paths in the flex circuits (which are mated by separable interposer contacts) are unequal and the fine end-lines are relatively lossy.

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Summary of Network Features

- Half of each H-block is without discontinuities
- Seven arms with three discontinuities each
- Seven vias; seven remote grounds; seven connectors
- **Discontinuities: $\Gamma_A \approx \Gamma_B \approx \Gamma_C \approx$ 0.15; 1.6 to 3.5 cm in length**
- All loads are $Z_0 // C_G$
- **All lines dispersively lossy, particularly end lines**
- C_G = 4 pF @ 50 MHz; 2 pF @ 100 MHz; 1 pF @ 200 MHz
- **τ_r = 0.5 ns, 50 MHz;** 0.25 ns, 100 MHz; 0.125 ns, 200 MHz

The important characteristics of the clock networks are summarized but the determination of these characteristics is saved for a later discussion.

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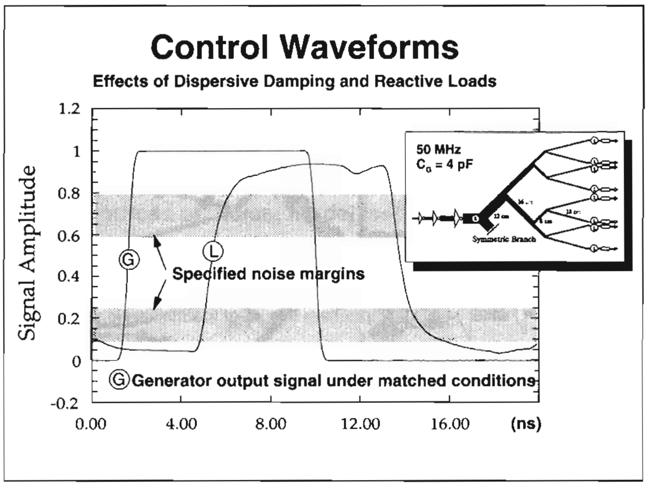

Propagation of signals is first simulated in order to observe the effects of frequency dependent loss, loss induced dispersion and the effects of reactive loads which are, for this purpose, capacitors placed in parallel with resistors $R = Z_0$.

The dominant effects are low level reflections at the fan-out points with mild dispersion, dispersive damping, mild propagation dispersion and dispersive loading which all combine to give the propagation modified waveform shown for 50 MHz. Similar waveforms are obtained for higher frequency clocks when C_G is correspondingly reduced and dispersive damping maintained at the same level. These constitute the control waveforms. The details of carrying out the simulation are discussed in the section on computational tools.

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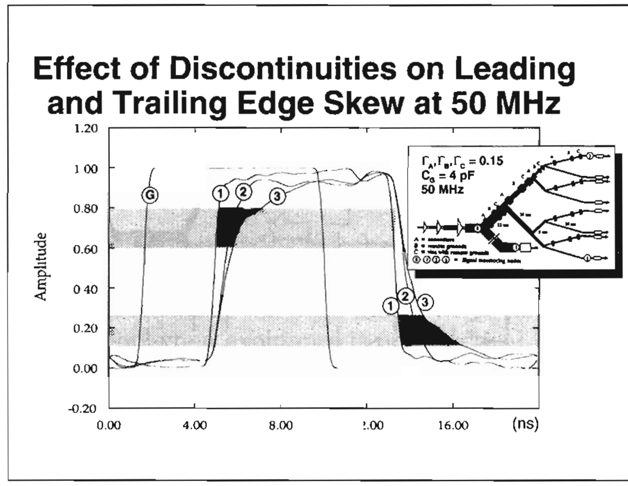

When the twenty one discontinuities corresponding to the preliminary design are introduced into one half of the network (as per design and product specifications), clock signals develop a leading edge skew ranging from 400 ps to 2 ns and a trailing edge skew ranging from 0.5 to 2.3 ns for 50 MHz operation. The degree of skew depends on the level within the noise margins that the devices are actually switching. The locus of skew at each edge is shown shaded.

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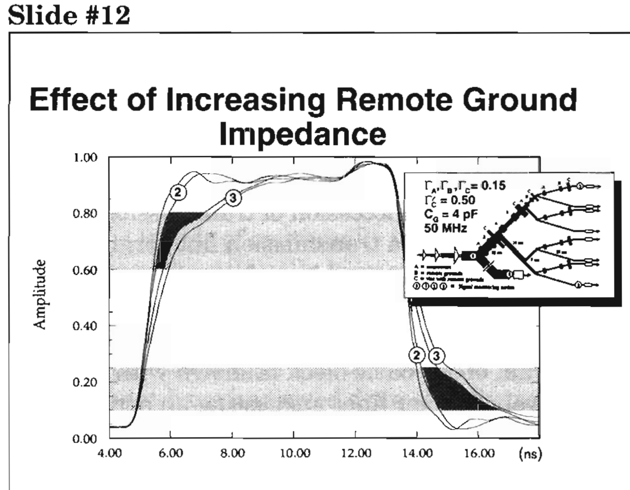

When only one of the connections Ⓒ in each branch is made to a more distant ground, increasing the reflection in the Ⓒ region to Γ_C=0.50, the observed skew between nodes ② and ③ nearly doubles at the leading edge and also increases substantially at the trailing edge. This is illustrated by comparing the waveforms obtained with Γ_C=0.15 to waveforms obtained when Γ_C=0.50. The shaded region between signals monitored at nodes ② and ③ corresponds to the locus of edge skew when Γ_C=0.15. When Γ_C=0.50, the waveforms monitored at nodes ② and ③ separate substantially as shown.

Problems of this type, both in clock distribution networks and in logic networks continue to increase in severity as clock rates continue to rise. Since interconnections are seldom perfect, other methods need to be developed to improve signal quality in high performance systems. For these reasons methods for noise management are discussed in the context of the resources required for the implementation of known and new techniques.

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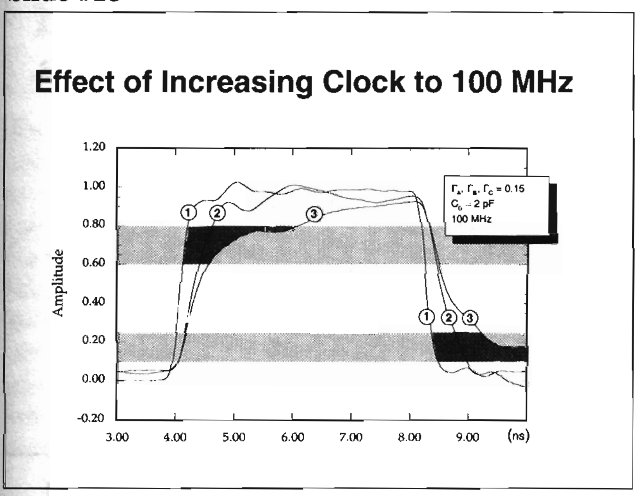

The skew effects are accentuated progressively as the clock rate is increased even though the device sizes are adjusted such that the device charging rate does not control the operating rate. Signal ① in all cases serves as a relative reference since it is monitored in the portion of the network which has no discontinuities.

The fraction of the period occupied by edge skew is continually increasing and the most degraded signal ③ is becoming marginally acceptable. Moreover, since signal distortions are not equivalent at leading and trailing edges, pulse skew also develops. For applications that use both edges of the clock and for applications that specify controlled duty cycle requirements, the effects of the discontinuities severely degrade the useful clock rate range of this network.

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Classification of Noise

Sources of noise \ Cures	Low loss lines	Load matching	Isolation	Reactive matching
Reflective @ load		●		◔
Reflective @ discontinuities				●
Crosstalk			●	◑
ΔI (w/ C_D)	◑			●
Ground shift (w/ C_D)	◑			◑

C_D ≡ decoupling capacitors

There are a number of causes for digital signal degradation. However, in practical systems, the many causes characterize more the physical description of the systems than the physical phenomena that cause signal noise. In systems being designed today all causes of noise are aggravated by impedance discontinuities and, therefore, can be cured or at least remedied by the reactive compensation techniques that form the subject of this paper. Particular attention is given to impedance mismatches created by such physical requirements as remote ground locations, ground loops, vias, bends, contacts, connectors, etc. which cause signal reflections at the respective locations, create the ΔI noise, accentuate the ground shift effect and accentuate crosstalk problems.

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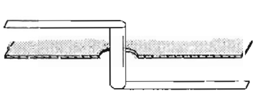
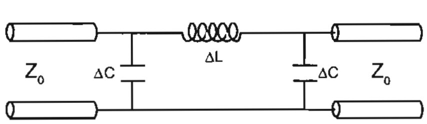
Circuit Models of Discontinuities



Signal path through a via changing level in a stripline structure

Bond wire on pads bridging microstrips



Approximate circuit model

Various features and technologies used for implementing the clock distribution described earlier are shown as component examples. At first, the usual models derived from circuital notions are shown for these components. The circuit models tend to emphasize the notions of excess capacitance and excess inductance.

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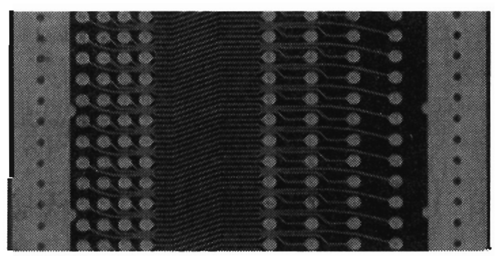
Flex Circuit Interconnections With Remote Grounding Contacts



The circuit illustrated above features bending and flexing qualities and a relatively high packaging density. The connections at the pads and the grounds are made with miniature separable contacts described later. Note that different signal connections are made with different distances to grounds which are shown as wide strips. Such remote grounds add high impedance sections to the controlled impedance signal paths which are along the lithographically produced microstrips.

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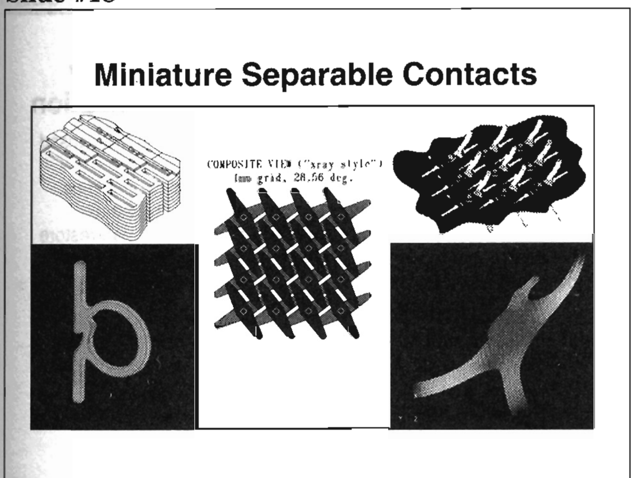

The flex circuit and other high density components such as multichip modules and large single chips are interconnected by unique, miniature, removable contacts used as interposers*. Interestingly, depending on the exact geometric configuration, these contacts can show high impedance, low impedance or impedance matched signal paths. In fact, some of the compensation principles described here were first used in the characterization of such separable assemblies which are electromagnetically relatively complex and are discussed later.

* MicroInterposer and Ampstar are the trademarks of AMP Incorporated for these contacts.

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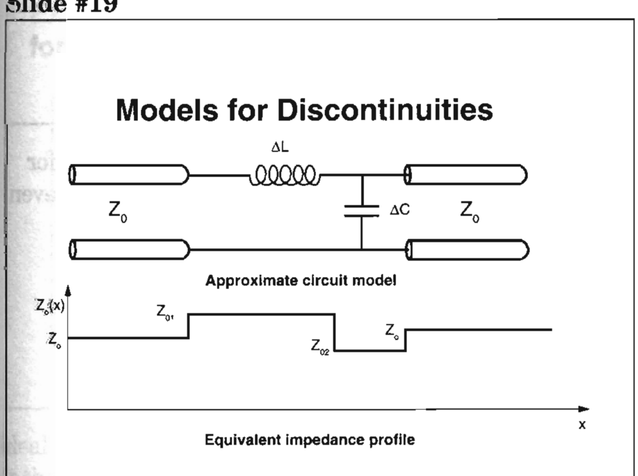

In a controlled impedance environment of a digital system, most signal transport occurs within some nominal characteristic impedance value Z_0.

However, in various regions of a system network, the physical arrangements may require such measures as providing extra lead length as in bringing a ground from a remote location or providing extra metal surfaces for establishing contacts. Generally, extra lead length introduces excess inductance and extra metal surface area introduces excess capacitance. We have become accustomed to think of excess inductance and capacitance as evil and we call them parasitics. There are some historic reasons for this attitude. We have learned in analog signal analysis in general and in microwave applications in particular that the frequency dependence of the reactance of an inductor is ωL and that the frequency dependence of the reactance of a capacitor is $1/\omega C$. Therefore, any excess of one or excess of the other is incompatible with digital signal propagation since it is well known that digital signals contain many frequencies which are unequally affected by the dispersive nature of these reactances.

All of this, of course, is true but it tends to send the wrong message and misleads us. In particular, referring to inductances and capacitances as parasitics sets an adversary relationship between those who lay out networks and design connectors and contacts and those who specify such requirements as minimum capacitance and particularly minimum inductance. For some reason, inductance has a terrible reputation. It must be partially because of the notoriety of the ΔI noise phenomenon.

In sum, this disposition sends the message that all inductance is bad and that all capacitance is bad and that we should all have less of each. Nothing could be further from the truth. In fact, it will be seen that in high performance systems when excess reactance of one type or the other exists, the system can be improved by adding reactance as a complement. These arguments hold both on an individual component level as well as on a system level.
The statistical implications at system level are particularly significant.

No rigorous proof is provided here for all the statements but even the heuristic arguments are more easily made and illustrated when any excess inductance is modeled as increased impedance and excess capacitance is modeled as lowered impedance as shown. The entire network can then be represented as a network of impedance profiles and their concomitant characteristics. Frequently, in electronic packaging, any excess reactance is somewhat distributed anyway and, therefore, showing it as a short section of transmission line is, in fact, more correct. The result of this modeling added to the requirements of incorporating other transmission line features reinforces the need for a simulator based fully on propagation principles as the one used to simulate the clock distribution network which will be discussed later.

This method of modeling and these considerations are helpful in formulating noise cancellation principles.

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Principles of Noise Cancellation by Reactive Compensation and Localization

- **Compensation:** Since electromagnetic reflections are caused by discontinuities in impedances and impedances are measures of the ratio between inductance and capacitance, it is suggested that restoring the ratio between the total inductance and total capacitance in a given region can restore the matching and eliminate reflections if conditions for relative localization can be satisfied.
- **Localization:** Relative localization can be achieved (even when the mismatched and the compensating regions are not coincident in space) when the total propagation time through the mismatched and the compensating regions is much shorter than signal risetime.

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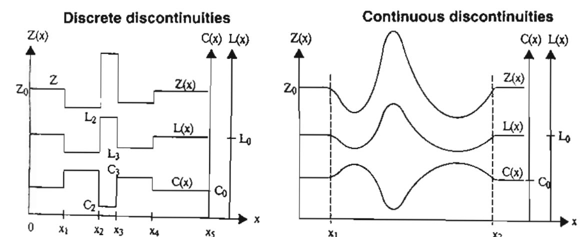
Compensation



$$\frac{\sum_{i=1}^{N}(x_{i+1}-x_i)L_i}{\sum_{i=1}^{N}(x_{i+1}-x_i)C_i} = Z_0^2 \qquad \frac{\int_{x_1}^{x_2} L(x)\,dx}{\int_{x_1}^{x_2} C(x)\,dx} = Z_0^2$$

The requirement for compensation can be stated for either distributed or discrete discontinuities and even discrete components.

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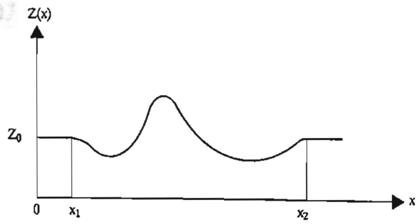
Localization



$\tau_r > 2\tau_p$

$\tau_p = (x_2 - x_1)\ \frac{\varepsilon_r}{V_0}$ = propagation time from x_1 to x_2

τ_r = signal risetime

When the condition for compensation is satisfied, noise cancellation is nearly complete when the signal risetime τ_r is greater than twice the propagation time τ_p through the discontinuity. It is important to note that noise cancellation continues to take place even when the localization condition is not satisfied well. However, the effectiveness of cancellation diminishes when $2\tau_p$ approaches or exceeds the value of τ_r.

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Example of Localization Design Rules for Partial Noise Cancellation (ε_r = 4.0)

Risetime, τ_r	Physical length in mm for ~ 90% cancellation	Physical length in mm for ~ 50% cancellation
1 ns	70	140
700 ps	50	100
500 ps	35	70
300 ps	20	40
100 ps	7	14
50 ps	3.5	7

Ideally, compensation should be done exactly at the location of the discontinuity. Then, when reactive compensation is complete, noise cancellation is complete. That is, wherever there is excess inductance, either the excess inductance should be removed or a corresponding amount of excess capacitance should be introduced. That's generally the easiest way to provide compensation when these principles are applied at a sufficiently early stage of design. The additional motivation is that, in any given geometry, inductance and capacitance have reciprocal relationships. Generally, by providing additional capacitance, inductance in that region is automatically reduced and conversely.

Of course, such absolute localization is seldom possible, especially with geometrically complex components. Then compensation should be provided within the shortest distance possible to the mis-matched region. For reflective noise, the amount of residual reflected energy is proportional to $2\tau_p/\tau_r$ where τ_p is the total signal propagation time through both the existing discontinuity and the compensation region and τ_r is signal risetime. Examples of physical lengths are given for ε_r = 4.00 for ~90% and ~50% noise suppression.

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Some Features of Reactive Matching

- Reactive matching applies to both discrete as well as distributed regions.
- Correlation effects provide additional favorable conditions for system level statistics.
- Unlike in situations where resistive matching must be used, reactive compensation is without signal penalty other than in possibly modifying propagation delay.

Since reactive components can return to the system all the energy they store, cancellation of noise by reactive compensation is, in principle, without penalty. But, because there are many ways of increasing the inductance to capacitance ratio, the effective propagation distance may change and, therefore, the effective propagation delay may be affected without an actual change in permittivity or permeability.

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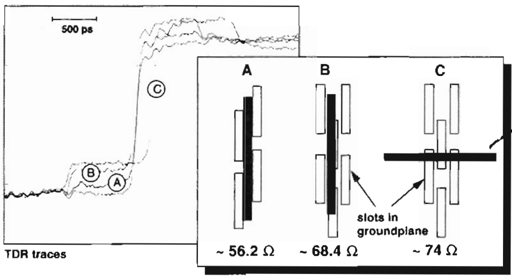
Example of Increasing Inductance and Its Effect on Signal Propagation Delay



As discussed before, reactive compensation techniques are without penalty except for possibly modifying propagation delay. This example serves to illustrate an untypical method for increasing the inductance to capacitance ratio of a microstrip or stripline without either changing the width of the strip or the strip to ground spacing. The connection is made on top of a ground plane perforated with elongated slots which create an anisotropic structure. In this case, the slots also serve as housings for the microinterposer devices described earlier.

Arrangements A, B, and C create progressively higher impedances as a result of modified ground currents and, for the same reason, produce different propagation delays. As seen on the TDR trace, structure B gives the shortest propagation delay and structure C gives a delay 45% longer than that of structure B. These are quite substantial effects, both on impedance and on propagation.

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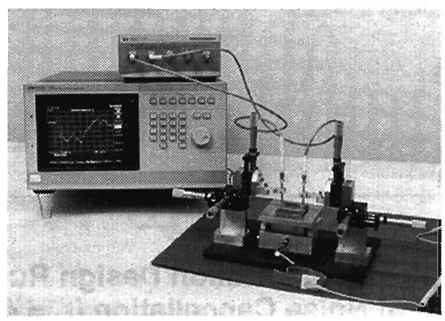
Frequency Domain Measurements on Network Analyzer



All time-domain measurements and verification of design are carried out on a time domain reflectometry system consisting of an HP 54121A Digitizing Oscilloscope, an HP 54121A Test Set for high speed pulse generation and sampling, an HP 9000, Model 310, computer controller which is networked with the HP-Apollo workstation ring by way of a LAN board and a Thin Ethernet Adaptor. This system is part of a substantial computational effort within which experimental time domain and spectral data can be merged with numerical analysis results for comparison, verification and validation. This facility is also networked directly to the National Center for Supercomputer Applications located near the laboratory.

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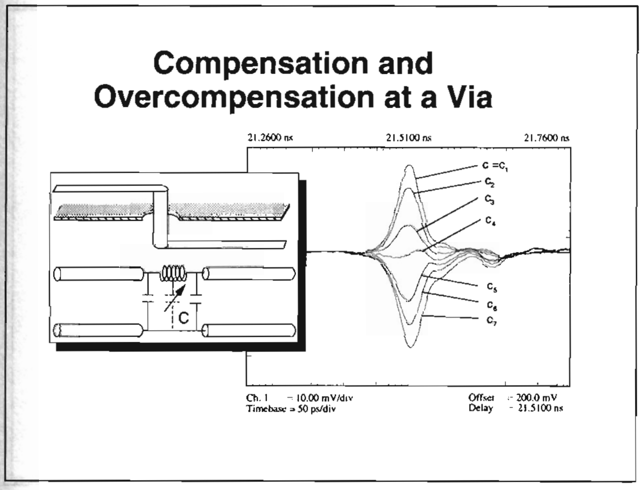

Compensation is very easily demonstrated on a prototype via in which the via region is left open such that additional grounding can be introduced, mimicking an increased capacitance such as produced by decreasing the via hole size. Because the via geometry is relatively small, localization is satisfied even for τ_r = 40 ps of the TDR system. The illustration shows the reduction and near cancellation of the positive reflected signal as capacitance is introduced into the region. As more capacitance is introduced, the via becomes a low impedance structure and gives a negative reflection.

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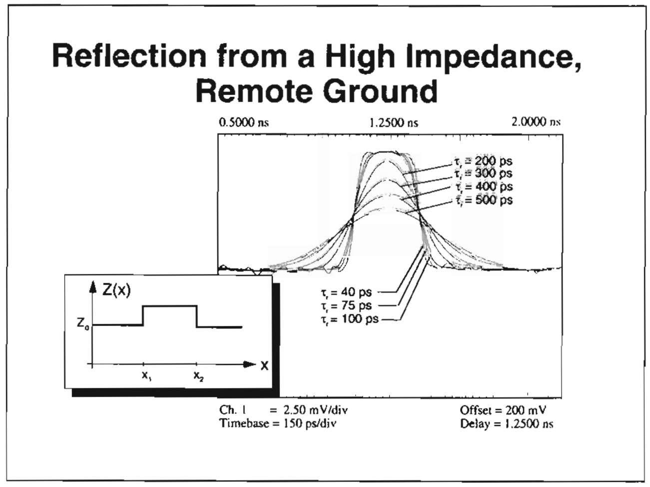

When a discontinuity is of high impedance, such as this remote ground connection of the flex circuit, the magnitudes of reflections from it do not change rapidly as the risetime of the signal is changed as shown on the traces of an HP TDR system. Thus, changing the risetime by more than a factor of ten spreads the reflection in time but reduces the peak magnitude only by a factor of less than two.

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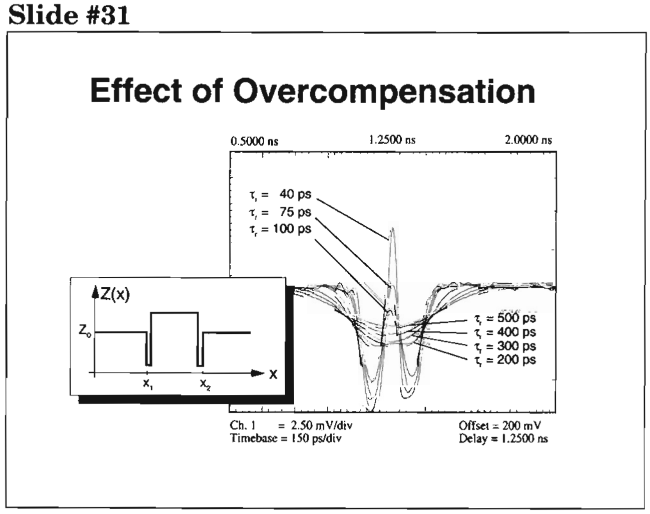

Similarly, when short sections of very low impedance are added at the ends, creating overcompensation, the reflection persists even for τ_r = 0.5 ns.

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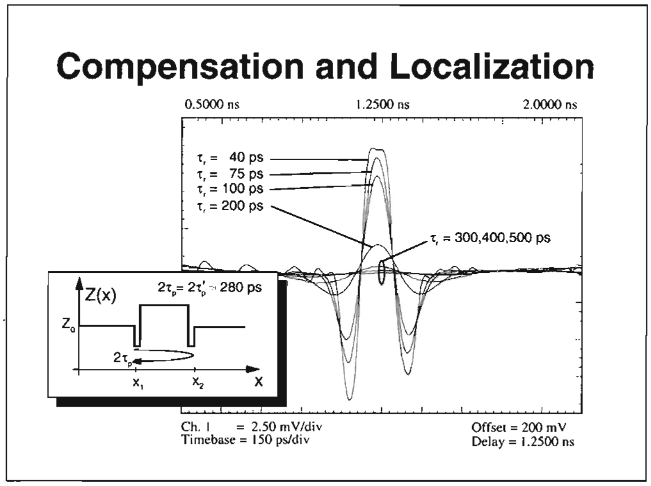

When compensation is of an appropriate amount, high speed signals still resolve the low impedance compensation and the high impedance remote ground. However, when the localization criterion is beginning to be satisfied such that the risetime τ_r starts exceeding $2\tau_p$, the reflection signal is reduced dramatically. Here, the overall length is approximately 3 cm in $\varepsilon_r \approx 2.1$ which gives $2\tau_p \approx$ 280 ps. Note that when τ_r is longer than ~ 300 ps, the reflection becomes very small and nearly vanishes when τ_r = 500 ps.

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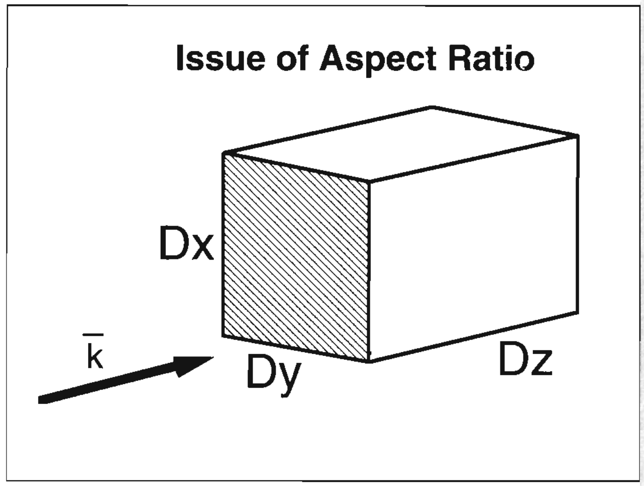

When the transverse dimensions Dx and Dy of an electronic interconnection are comparable to the longitudinal dimension Dz over which the object has a uniform cross section, neither static nor quasistatic principles are adequate to predict its performance for high speed applications. Many packaging features and components fall into that category, requiring a full wave, 3D-electromagnetic vector solver.

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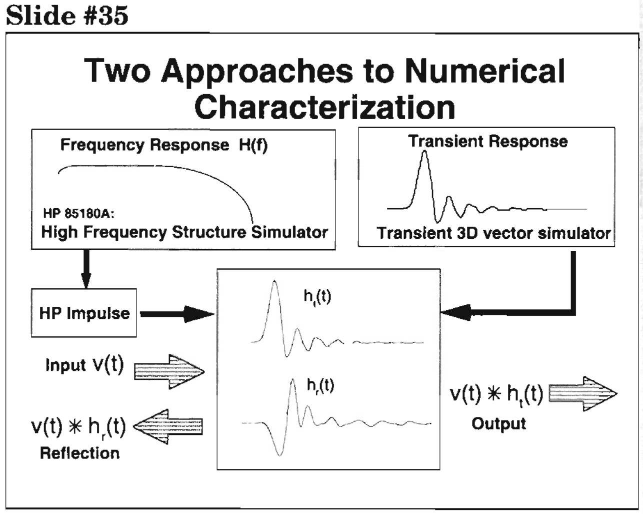
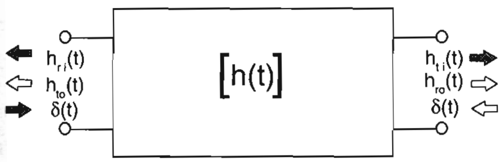


Whether the electromagnetic structure solver is based on harmonic analysis or transient analysis, the most convenient approach consists of obtaining an impulse transfer function from which the response to any waveform can be obtained by convolution.

Slide #36

Transfer Function System Simulation of Digital Networks



$$\begin{bmatrix} v_i(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} h_{ri}(t) & h_{to}(t) \\ h_{ti}(t) & h_{ro}(t) \end{bmatrix} * \begin{bmatrix} v_{ii}(t) \\ v_{io}(t) \end{bmatrix}$$

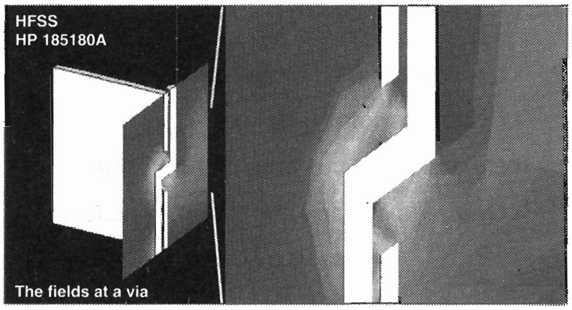
System simulation consists of a sequence of convolution integrals

An interconnecting structure can be entirely characterized by obtaining the transmitted and reflected waveforms to impulse inputs. Impulse inputs $\delta_i(t)$ and $\delta_o(t)$ are numerically generated at both ends of the structure and the transmitted responses h_{ti} and h_{to} and the reflected responses h_{ri} and h_{ro} are determined. This method of characterization defines the reflective and transmitting signal response properties of a component and provides an analytical description suitable for the simulation of a network of components.

Thus, for numerical evaluation of the performance of different packaging technologies and methods, both an electromagnetic component characterization tool and a network simulation tool are required.

Slide #37

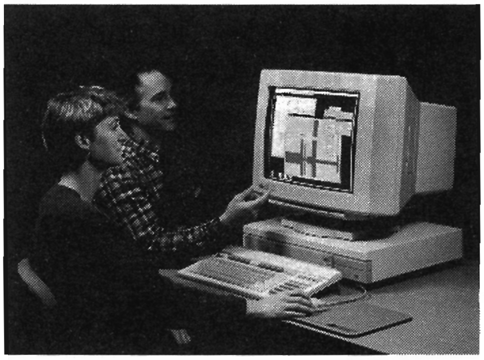
High Frequency Structure Simulator



A broad menu of options is available with the HP High Frequency Structure Simulator (HFSS), HP 85180A, including transfer of files to HP Impulse for the determination of the impulse responses and for subsequent time domain analysis.

Slide #38

Measurement Setup: TDR



With HFSS, solutions can be obtained for S-parameters, propagation constants, impedance, etc. It can give single frequency results or it can be operated in a sweep mode. Clearly, the frequency data of HFSS are the natural complements to network analysis data that is obtained on an HP 8720/8510 Network Analyzer and the time-domain data of HP Impulse are the natural complements to TDR results.

Slide #39

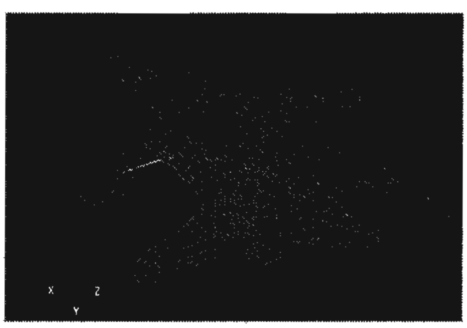
Transient 3D-Vector Simulator Features

- Launch impulse or any waveform
- Obtain transfer functions
- Convolution and post computations
- Graphics of currents, fields, waveforms

The transient simulator gives directly the impulse response and shows directly the distribution of fields when a time domain signal propagates through it. This is not a commercial product but is one of the tools used for characterizing microelectronic packaging products or design of new products in cooperative projects with industry.

Slide #40

Geometry of Interconnections Made with Interposer* Contacts



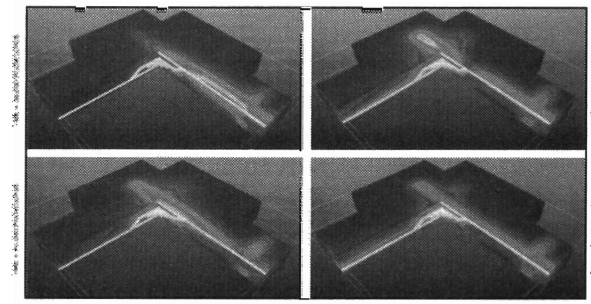
* Ampstar is a trademark of AMP Incorporated for this separable contact

The dynamics of a full wave 3D transient solver is illustrated on a set of interposer connections.

The geometry of the interconnections consists of one star contact for connecting the strips of two microstrips and one star contact (foreground) for connecting the grounding pads which are connected to the ground planes by vias. (The vias are shown as posts of square cross section for computational reasons). The ground planes and the dielectric supporting the strips are not shown for clarity.

Slide #41

Example of Select Frames of a Transient 3D Simulation

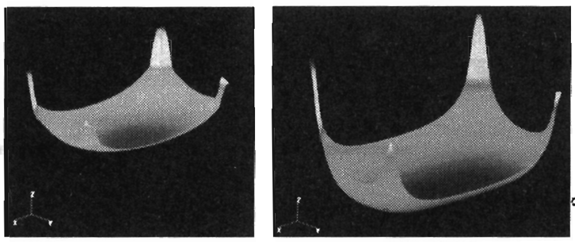


The select frames show the fields developing at the contacts as the signal is approaching. The fourth frame shows a striking example of the field concentration at the tip of the contact as a positive reflection adds to the incoming wave.

Both HFSS and the transient simulator shown here take into account all aspects of the geometric complexity without approximations other than the discretization of space.

Slide #42

Current Penetration Into Conductors



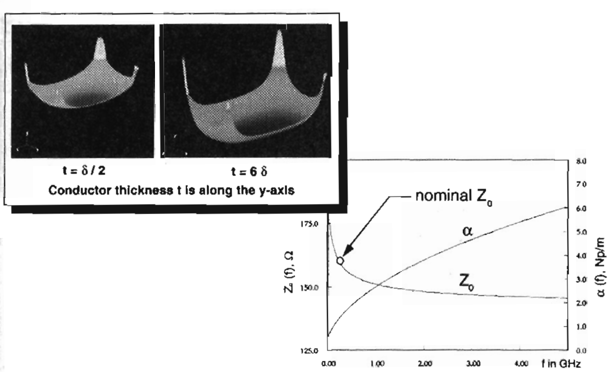
t = δ / 2 t = 6 δ

Conductor thickness t is along the y-axis

For particularly small conductors and in the presence of high frequencies, variations of the propagation parameters α, β and even the variation of the characteristic impedance Z_0 with frequency may be sufficiently significant to affect the resultant network signal. The particularly thin traces of the 18 cm, end-lines of the H-block network show the characteristics illustrated here.

Slide #43

Conductor Loss



When cross sectional dimensions of conductors are comparable to current penetration depth, detailed current distributions need to be obtained before $\alpha = \alpha(\omega)$, $\beta = \beta(\omega)$, and $Z_0 = Z(\omega)$ can be determined. Depending on the type and quality of metal traces or leads, current depths in conductors vary. For copper, depending on it's quality, current penetration can range from nearly a mil at 50 MHz to below a micron for ~ 5 GHz harmonics.

Examples are shown of the manifestation of the classical skin effect when current penetration depth is comparable to cross sectional dimensions of the conductor. Even when current penetration δ is substantial, δ = 2t, conductor edges and corners carry a significant amount of current. When penetration is small, δ = t/6, a very large proportion of current is carried by the corners and edges.

Slide #44

Network Simulator Features

- **Based entirely on propagation principles**
- **Takes into account dispersive and nondispersive:**
  - — propagation: $\beta = \beta(\omega) \Leftarrow \alpha \neq 0$; $\beta = \beta(\omega) \Leftarrow \varepsilon_{eff} = \varepsilon_{eff}(\omega)$
  - — damping with dispersive loss: $\alpha = \alpha(\omega)$
  - — reflections with $\Gamma = \Gamma(\omega)$
  - — distributed or discrete discontinuities or components
  - — linear, nonlinear loads
  - — cross talk: dielectrically homogeneous, inhomogeneous
- **Post-simulation analysis and graphics**

After all the components of the intended technologies have been characterized, either analytically (HP HFSS, HP Impulse, Transient 3D, Current Profile) or with instruments (TDR, network analysis), the intended network is constructed for performance evaluation. Again, evaluation can be on a prototype network or with computer aided simulation.

In order to assess the effectiveness of a network design or the effectiveness of various improvements by analytical means, a network simulator capable of including all significant effects is required. For this case study, the clock distribution network is entered into a simulator based entirely on propagation principles and capable of taking into account all the propagation effects of a complex network, including propagation, damping, reflections, distributed as well as discrete discontinuities and fan-in and fan-out. Moreover, all aspects of propagation, damping, reflections and loading can be dispersive such as in lossy lines or dielectrically inhomogeneous lines and in reactive loading. Provisions are also in place to take into account crosstalk in dielectrically homogeneous and inhomogeneous networks. This simulator is also not a commercial product but is again one of the analytical tools used in joint projects with industry.

Slide #45

Noise Cancellation in System Packaging

I. System noise: a case study

II. Sources of noise; model issues; technologies

III. Principles of noise cancellation

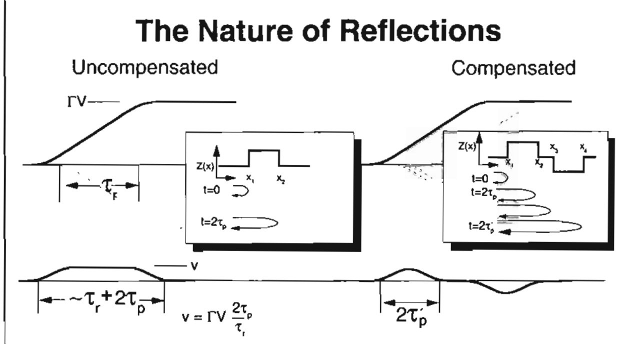
IV. Characterization and compensation

A. Measurement tools and methods

B. Advanced computational tools

V. Case study: use of noise cancellation

Slide #46

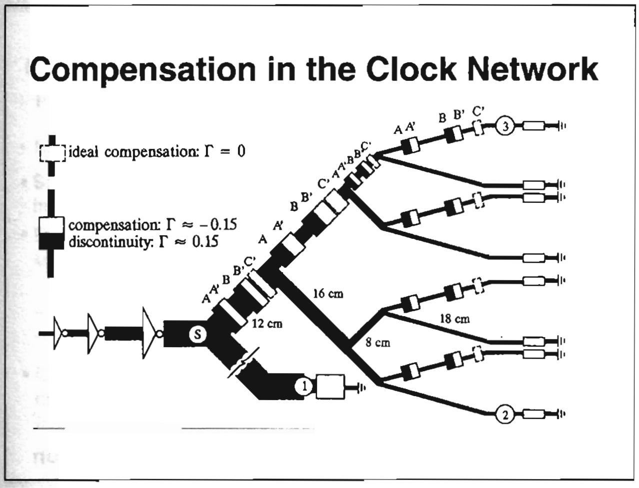


Equal and opposite polarity reflections are generated by the trailing edge

The effect of reactive compensation and noise cancellation was illustrated on individual components by making use of TDR instruments. The collective and statistical effects are best illustrated by implementing compensation on an entire network and evaluating its effectiveness with the network simulator.

The statistical implications of compensation are best illustrated by reviewing graphically the features of the reflections under compensated and uncompensated conditions. The duration of a reflection from a reactive discontinuity corresponds to the sum of the risetime of the signal τ_r and twice the propagation time τ_p through the discontinuity. That is, even a short discontinuity gives a reflection as long in duration as the risetime of the signal. In contrast, the duration of a reflection for a compensated network for which the localization criterion is met is on the order of $2\tau_p$ where τ_p is the propagation time through both the existing discontinuity and the compensating discontinuity. This is, of course, the worse case since it assumes that no overlap is possible between the discontinuity and the compensating region. What is significant is that in compensated structures an equal and opposite polarity reflection follows within τ_r. These characteristics have substantial implications for statistical analysis of system noise content.

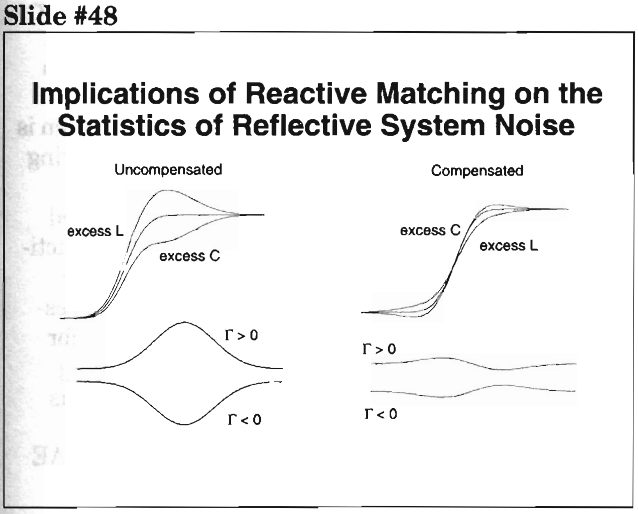
Slide #47



Returning to the clock distribution network, it was seen that the problems of skew were increasing with increasing clock rate. In order to illustrate the noise cancellation technique, the networks are modified as follows.

The remote grounds C are entirely eliminated and redesigned to conform to controlled impedance signal paths. The connectors B, however, and the vias A with remote grounds could not be eliminated or modified. For compensation, each high impedance of A and of B is followed by a low impedance A and B of similar length.

Slide #48



Even though the cancellation of reflective noise is incomplete when localization is imperfect, there is a secondary statistical advantage to the implementation of reactive matching since, as already illustrated, the residual components appear as equal pairs of opposite polarities. That is, when compensation is complete but τ_p is not zero (incomplete localization), every residual reflection is accompanied by an equal and opposite residual reflection within each edge of each signal. When a statistical distribution of such residual components exists in both amplitude and time, the overall effect is that of further noise cancellation regardless whether the initial discontinuities are all inductive, all capacitive or a mixture of both.

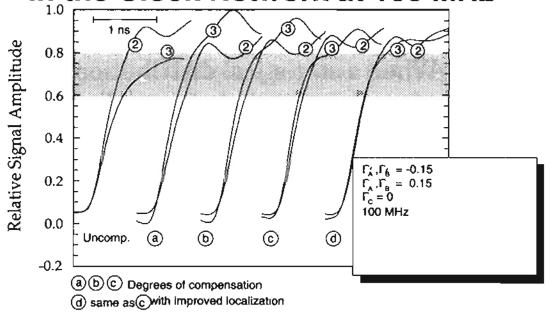
When uncompensated discontinuities are dominated by high impedance such as remote grounds, vias, wire bonds, etc., all reflective noise from leading edges is additive and is positive and all reflective noise from trailing edges is additive and is negative. The converse is true when uncompensated discontinuities are dominated by capacitive discontinuities.

Therefore, when no reactive compensation is provided, favorable statistical effects occur only when the reflective noise is statistically scattered over a time interval as large as the clock period T.

In contrast, when compensation is implemented, reflective noise needs to be statistically distributed only over an approximate time interval of $2\tau_r$ for favorable statistical effects to exist. The other circumstance which can show statistically favorable cancelling effects without providing compensation is when there is an equivalent mix and statistical distribution of high and low impedance discontinuities. Of course, that is simply a statistical statement of compensation.

Slide #49

Cancellation of Skew by Compensation in the Clock Network at 100 MHz



The effectiveness of introducing distributed compensating discontinuities for noise cancellation is illustrated by providing different degrees of compensation. Illustrations are for leading edges only, for simplicity. Comparing the leading edges of (a) to the uncompensated edges, it is seen that the network is first overcompensated since waveforms (2) and (3) switch order. Waveforms (b) and (c) show improved degrees of compensation. Significantly, waveforms (a), (b) and (c) correspond to progressively improved compensation but the localization criterion is not met very well, particularly in the end lines. However, when compensation is placed in the end lines in such a way as to introduce compensation at the centers of the discontinuities (effectively decreasing all discontinuity lengths by a factor of two) waveform (d) is obtained which shows a nearly total elimination of skew in the leading edge. Signal quality is similarly improved at the trailing edges.

The statistical cancellation effects are dramatically illustrated by these waveforms since on a component by component basis a much greater attention to detail would have been required, especially regarding relative localization, for good cancellation to have taken place.

Slide #50

Summary

- **Reactive mismatching**
  - — dominates signal degradation
  - — lends itself to noise cancellation
- **Cancellation**
  - — requires compensation: a budget of ΔZ
  - — requires localization $\tau_r > 2\tau_p'$
  - — can be complete or achieved as a trade-off
  - — applies to discrete, continuous mismatch
  - — applies to logic, clock, power distribution
  - — is without signal penalty
  - — favorably enhanced by statistical effects
- **High performance achieved with noise cancellation**

Substantial improvements in signal quality both at component level and system level can be achieved by appropriately balancing the reactive design of digital networks. Proposed measures apply equally to logic, clock, and power distribution networks. In order to develop the needed criteria, methods for signal propagation analysis and testing in microelectronic digital networks are summarized and dominant issues relating to digital signal degradation are reviewed. Sources of noise are identified and characterized with particular attention being given to reflective noise caused by reactive mismatching such as remote grounds, vias, connectors, ground loops, etc. It is shown that with the exception of device loading, reactive mismatching is the dominant source of signal degradation in many digital networks that are being designed today. Principles for reactive compensation and criteria for localization are developed and explained in the context of high speed digital operation. It is shown that unlike in cases of resistive matching, reactive compensation is without signal penalty other than possibly effecting a modified signal propagation delay. Dramatic improvements in signal quality are demonstrated for a number of examples. Design criteria for practical reactive matching are developed based on the degree of desired compensation and noise suppression. Guidelines for reactive noise cancellation for digital systems operating with risetimes ranging from several nanoseconds to risetimes as short as 50ps are given. Case studies of vias, bends, and interposer contacts are used for illustration of CAE and test tools.

A system perspective is developed and the effects of reactive compensation on the statistics of system noise are discussed and illustrated.

Slide #51

Conclusions / Recommendations

For achieving high performance at system level

- Early attention to technologies (semiconductor, packaging)
- Selection of vendors and suppliers capable of implementing advanced concepts
- Rich environment of advanced tools

MEASUREMENT	ANALYTICAL
— multiple channel TDR	— 3D vector modeling
— LCZ	— impulse characterization
— network analysis	— simulation based on propagation

- Controlled impedance design with noise cancellation concepts on all networks including power distribution for ΔI suppression

Slide #52

Recommended Resources

- Equipment and accessories
  - — HP 54121T TDR Oscilloscope
  - — HP 8720/8510 Network Analyzer
  - — Probe stations and fixtures
- Simulation Tools
  - — HP HFSS
  - — HP MDS/Impulse
- Consultant services
  - — 3D characterization
  - — Current density characterization: loss/dispersion
  - — Advanced network simulation; supercomputations
  - — System packaging, design, seminars

They have HFSS + one other field solver
with AHP they modeled the interposer