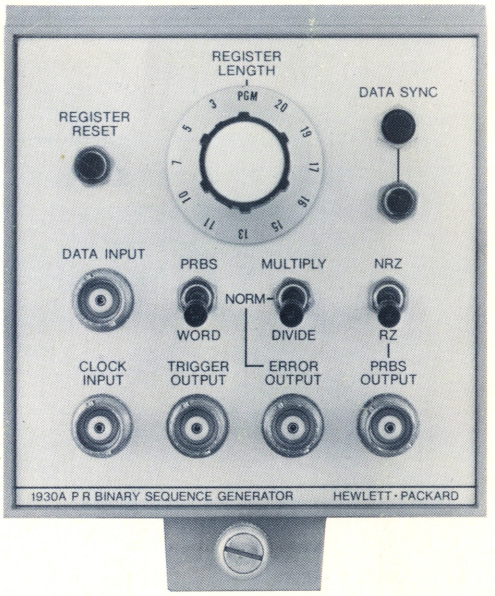
OPERATING AND SERVICE MANUAL

PSEUDO RANDOM BINARY SEQUENCE GENERATOR

1930A



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CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

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OPERATING AND SERVICE MANUAL

MODEL 1930A PSEUDO RANDOM BINARY SEQUENCE GENERATOR

SERIALS PREFIXED: 0987A–

Refer to Section VII for instruments with other Serial Prefixes.

HEWLETT-PACKARD COMPANY/COLORADO SPRINGS DIVISION
1900 GARDEN OF THE GODS ROAD, COLORADO SPRINGS, COLORADO, U.S.A.

Manual Part Number 01930-90901.
Microfiche Part Number 01930-90801.

PRINTED: FEB 1971

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides operating and servicing information for the Hewlett-Packard Model 1930A Pseudo Random Binary Generator (Figure 1-1). The manual is divided into eight sections, each covering a specific topic or aspect of the instrument. All schematics are located at the rear of the manual and can be unfolded and used for reference while reading any part of the manual.

1-3. This section contains a description of the Model 1930A. The instrument specifications are listed in Table 1-1.

1-4. DESCRIPTION.

1-5. Model 1930A is a digital data generator. The format of the pseudo-random binary sequences (PRBS) generated can be either return-to-zero (RZ) or non-return-to-zero (NRZ). Repetition rates up to 40 MHz (typically 50 MHz) can be attained. The length of the sequence of ones and zeroes can vary from 7 to 1,048,575 bits before being repeated. Model 1905A or 1906A rate generator plug-ins provide clock rates of either 25 or 50 MHz, and the output pulses can be shaped by any of the 1900-system output stages. Model 1917A provides control of TTL levels. ECL and bi-polar pulses can be generated with Model 1921A or 1922A output stages.

1-6. Electronic DTL/TTL compatible programming allows complete choice of feedback taps and the generator polynomial. With programming, any of the 73,080 different possible maximal length sequences may be generated along with about one million non-maximal length sequences. To program the Model 1930A, it must be installed in a 1900-series mainframe equipped with Option 001, the programming option.

1-7. A Model 1930A sequence is random in that it closely follows the statistical characteristics of a binomial distribution for samples of N bits or less (where N is the shift register length) and is pseudo-random since it is deterministic and periodic. These pseudo-random sequences provide a tool for testing every area of generating, handling, transmitting or processing binary signals. Three major applications for the Model 1930A are: random signal simulation, bit error detection and digital cryptography.

1-8. Random signal simulation allows a device that processes digital information to be completely exercised while providing the stationary characteristics of a repetitive signal. In pattern sensitive devices, pseudo-random binary sequences provide a fast, easy, complete method to generate all possible combinations of up to 20 bits during design and check-out. Also, in an N cell device, a random sequence can be generated that is 2^N-1 bits long that contains all possible combinations of N bits except the all-zero combination.

1-9. Bit error detection in digital transmission systems is simplified by the ability of the Model 1930A to rapidly synchronize to a data stream (either words or pseudo-random sequences) and do a bit-by-bit comparison of the incoming data. For example: one Model 1930A generates a signal that is transmitted over a digital communications link and a second Model 1930A would then synchronize to the incoming signal from the digital link. Each time the received signal is different from the stored replica an error pulse is produced at the error output, which can be counted to provide a bit error rate measurement.

1-10. Cryptography in digital applications is accomplished by dividing the incoming data stream by the characteristic equation of the generator. The pseudo-random binary sequence completely scrambles the original data in both time and frequency domains. Eleven different scrambling patterns can be selected with the front-panel register length switch, and feedback taps inside the plug-in provide for the selection of over 73,000 different pseudo-random patterns. To decode the information, another Model 1930A, set to the same sequence, multiplies the scrambled signal by the same equation to regain the original data.

1-11. WARRANTY.

1-12. The instrument is certified and warranted as stated on the inside front cover of this manual.

1-13. ACCESSORIES.

1-14. Plug-in board extender (HP Part No. 5060-0459) is furnished with Model 1930A as a troubleshooting aid. A complete line of test equipment cables, connectors, adaptors and other test and accessory items are available but not furnished. For information on specific items, refer to the HP Catalog or contact the nearest Hewlett-Packard Sales/Service Office.

1-15. INSTRUMENT AND MANUAL IDENTIFICATION.

1-16. This manual applies directly to Model 1930A instruments with a serial prefix number as listed on the manual title page. The serial prefix number is the first group of

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains instructions for performing an initial inspection of the Model 1930A. Installation procedures and precautions are presented in step-by-step order. The procedure for making a claim for warranty repairs and for repacking the instrument for shipment are also described in this section.

2-3. INITIAL INSPECTION.

2-4. The instrument was inspected mechanically and electrically before shipment. Upon receipt, inspect it for damage that may have occurred in transit. Check for broken knobs, bent or broken connectors, and dents or scratches. If damage is found, refer to the claims paragraph in this section. Retain the packing material for possible future use.

2-5. Check electrical performance of the instrument immediately after receipt. Refer to Section V for the performance check procedure. The performance check will determine whether or not the instrument is operating within the specifications listed in Table 1-1. Initial performance and accuracy of the instrument are certified as stated on the inside front cover of this manual. If the instrument does not operate as specified, refer to the claims paragraph in this section.

2-6. PREPARATION FOR USE.

2-7. The Model 1930A is shipped ready for immediate use. Mounting, power requirements, cooling and instrument compatibility are discussed in the following paragraphs.

2-8. INSTRUMENT MOUNTING.

2-9. The Model 1930A will fit into any one of the four compartments in a 1900-series mainframe. It's position in the mainframe will be determined by the other plug-in instruments being used in the mainframe and by the desired interfacing.

2-10. The instrument is mounted by inserting it into the selected compartment. The two plugs on the rear of the instrument will engage two jacks in the mainframe with moderate pressure applied. After the plugs are seated, tighten the panel fastener finger tight.

2-11. POWER REQUIREMENTS.

2-12. Certain combinations of 1900-series plug-ins may overload a Model 1900A Mainframe. For instance, not more than two Model 1930A instruments may be used in a Model 1900A. If three or four Model 1930A instruments must be used in a single mainframe, the Model 1901A must be used.

2-13. INSTRUMENT COOLING.

2-14. Cooling for the Model 1930A is provided by the 1900-series mainframe. The operating temperature will be adequately controlled if the instructions found in Section III of the 1900-series Operating and Service Manual are followed.

2-15. INSTRUMENT COMPATIBILITY.

2-16. As long as the limitations in paragraph 2-12 are observed, the Model 1930A will be compatible with any other 1900-series plug-in instrument whose function is compatible with the applications of the Model 1930A.

2-17. CLAIMS.

2-18. The warranty statement applicable to this instrument is printed inside the front cover of this manual. If physical damage is found, or if operation is not as specified when the instrument is received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office immediately (refer to the list in back of this manual for addresses). The HP Sales/Service Office will arrange for repair or replacement without waiting for settlement of the claim with the carrier.

2-19. REPACKING FOR SHIPMENT.

2-20. If the Model 1930A is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and description of the service required.

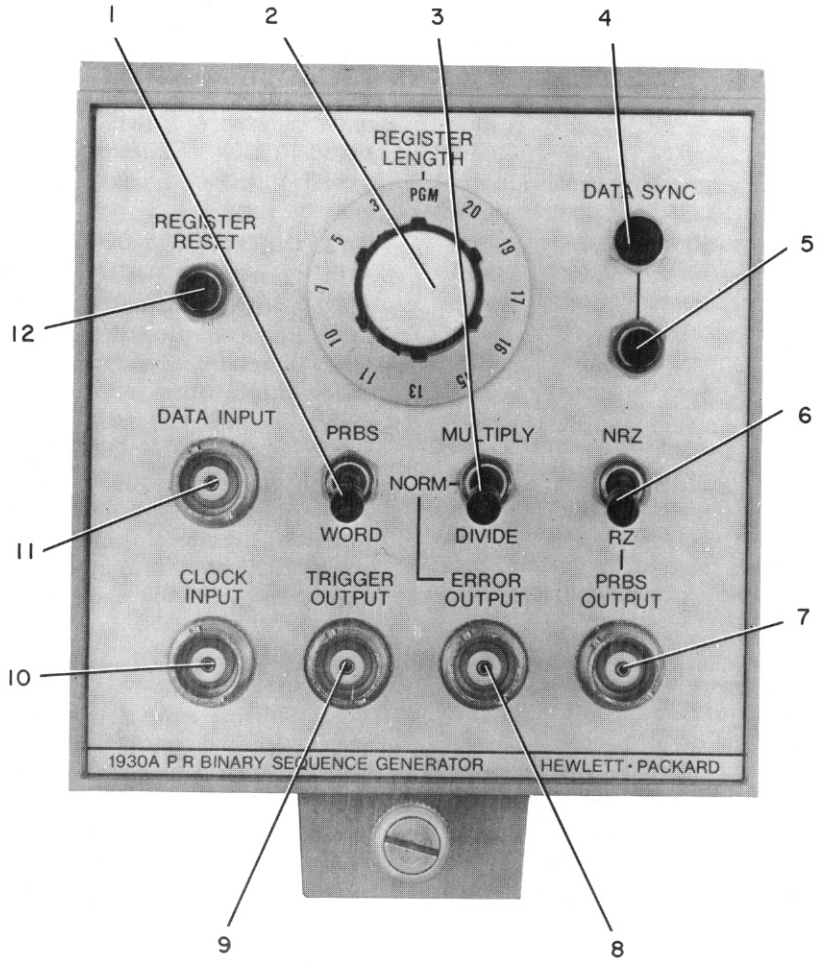
2-21. Use the original shipping carton and packing material. If the original packing material is not available, the HP Sales/Service Office will provide information and recommendations on materials to be used. Materials for shipping an instrument normally include the following:

a. A double-walled carton with 200 lb test strength.

b. Heavy paper or sheets of cardboard to protect all instrument surfaces: use a nonabrasive material such as polyurethane or cushioned paper such as Kimpak around all projecting parts.

c. At least 4 inches of tightly packed, industry-approved shock-absorbing material such as extra-firm polyurethane foam.

d. Heavy-duty shipping tape for securing outside of carton.



1. PRBS/WORD. Changes operation of shift register between closed loop shift register and PRBS generator.

2. REGISTER LENGTH. Electronically changes length and feedback taps of the shift register.

3. MULTIPLY/NORM/DIVIDE. Switches between decode, normal PRBS and encode.

4. DATA SYNC. (Lamp). Indicates data synchronization when lighted.

5. DATA SYNC (switch). When pressed, causes data synchronization.

6. NRZ/RZ. Changes output format between non-return-to-zero and return-to-zero.

7. PRBS OUTPUT. Shift register output connector.

8. ERROR OUTPUT. Error pulse output connector.

9. TRIGGER OUTPUT. Trigger pulse output connector.

10. CLOCK INPUT. Clock input connector.

11. DATA INPUT. Data input connector.

12. REGISTER RESET. Causes all cells to reset to zero.

1930A-A-9

Figure 3-1. Front Panel Controls and Connectors

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section provides information covering operation of the Model 1930A. It provides the required operating considerations, a description of the functions of the front panel controls, and instructions for front panel control of the instrument. It also provides instructions for electronically programing the instrument.

3-3. OPERATING CONSIDERATIONS.

3-4. CLOCK.

3-5. The Model 1930A requires an external clock source. For best results, the clock source should be a pulse generator capable of outputs of 1 to 4 volts when terminated in 50 ohms, with repetition rates up to 60 MHz. The HP Model 1906A fills these requirements.

3-6. INTERFACE SWITCHES.

3-7. The Model 1930A is equipped with two interface switches, located internally on the left-hand side of the instrument. The switches permit routing of the CLOCK INPUT and the PRBS OUTPUT signals through selectable 1900-series mainframe transmission lines instead of the front-panel connectors. When the interface switches are set in the forward position, the CLOCK INPUT and PRBS OUTPUT signals are applied through the front-panel connectors. When the interface switches are set to the rear position, the signals are routed through the plug-in connector of the instrument and the 1900-series mainframe inner-compartment connectors. Check to ensure proper connections between the inter-compartment connectors in the mainframe before inserting the Model 1930A.

3-8. FUNCTION DESCRIPTION.

3-9. To enable the operator of the Model 1930A to better understand the operation of the instrument controls, a brief description of some of the circuit functions follow. For more detailed circuit explanations, refer to Section IV.

3-10. Basically, the Model 1930A is a shift register with the required input circuits, output circuits and feedback and mode controls. The shift register consists of 20 cells. Each cell consists of a flip-flop, an input gate and a feedback gate.

3-11. In order to generate pseudo-random binary sequences (PRBS) each shift register cell has been provided with a means of connecting it's input with the output of the first cell. These connections are called feedback taps. The feedback taps may be connected in two ways. First, by internal diode logic which is activated by the REGISTER LENGTH SWITCH. Second, by switching the REGISTER LENGTH switch to PGM and signaling the connections with remote electronic programing.

3-12. By setting the PRBS/WORD switch to WORD, the shift register is able to synchronize with externally generated binary words of length N. By setting the switch to PRBS the shift register is able to generate or synchronize PRB sequences of length $2^N - 1$. In both cases N is equal to the setting of the SHIFT REGISTER switch. For instance, if the REGISTER LENGTH switch is set to 5 and the PRBS/WORD switch is set to PRBS, then feedback taps 3 and 5 (see Table 3-1) are activated and a PRB sequence 31 ($2^5 - 1$) bits long is generated.

Table 3-1. Commonly Used Feedback Configurations

Register Length	Feed Back Taps	Sequence Length
2	1, 2	3
3*	2, 3	7
4	3, 4	15
5*	3, 5	31
6	5, 6	63
7*	6, 7	127
8	2, 3, 4, 8	255
9	5, 9	511
10*	7, 10	1023
11*	9, 11	2047
12	2, 10, 11, 12	4095
13*	1, 11, 12, 13	8191
14	2, 12, 13, 14	16383
15*	14, 15	32767
16*	11, 13, 14, 16	65535
17*	14, 17	131071
18	11, 18	262143
19*	14, 17, 18, 19	524287
20*	17, 20	1048575

(*) available at front panel on REGISTER LENGTH switch.

3-13. CONTROLS AND CONNECTORS.

3-14. Front panel controls and connectors are identified and described briefly in Figure 3-1. A more detailed description is given in the following paragraphs.

3-15. DATA INPUT.

3-16. The input data will consist of externally generated binary words or PRB sequences. The data may be added to or compared with the contents of the shift register.

3-17. MULTIPLY/NORM/DIVIDE.

3-18. NORM. In this configuration, the data input will be compared with the output of the shift register. If the two signals are different, an error pulse will be delivered at the ERROR OUTPUT.

3-19. DIVIDE. In this configuration, the data input will be added into the shift register. This results in the data input being scrambled in a manner determined by the shift register feedback taps. Mathematically, the data will be divided by the characteristic equation of the shift register circuit.

3-20. MULTIPLY. In the absence of input data, the shift register will generate binary words according to the configuration of the feedback taps.

3-21. When input data is present at DATA INPUT, it will be added into the shift register. Mathematically, the data will be multiplied by the characteristic equation of the shift register circuit. If the input data (as received at DATA INPUT) has been scrambled in the DIVIDE mode in another Model 1930A, it will be unscrambled in the MULTIPLY mode. This results in a complete encode/decode operation.

3-22. DATA SYNC. (switch)

3-23. When pressed, this switch causes synchronization of the contents of the internal shift register with an externally generated binary word or PRB sequence applied to DATA INPUT, provided that the characteristic equation or feedback structure of the external generator matches that of the Model 1930A. If the external generator is another Model 1930A, a Model 1925A or a Model 3722A, the feedback structures will be identical for the same length binary word or PRB sequence and synchronization can take place.

3-24. DATA SYNC. (lamp)

3-25. If the data input and PRBS output are the same for greater than one second, the DATA SYNC lamp will light indicating synchronization.

3-26. PRBS/WORD.

3-27. WORD. In this mode, the contents of the shift register will be continously cycled with a period equal to the shift register length.

3-28. PRBS. In this mode, other feedback taps are provided to generate pseudo-random binary sequences.

3-29. REGISTER LENGTH.

3-30. This switch selects 11 commonly used binary words or PRB sequences according to the position of the PRBS/WORD switch. When set to PGM it enables the electronic programing feature of the Model 1930A.

3-31. RZ/NRZ.

3-32. This switch selects the format of the PRBS output signal. In NRZ, a one is represented by a high level and a zero by a low level. With RZ selected, a one is represented by a pulse whose width is equal to the width of a clock pulse, and a zero by the absence of a pulse. The RZ pulse may be shaped by an output stage such as HP Models 1915A, 1917A, 1921A or 1922A.

3-33. CLOCK INPUT.

3-34. The basic timing signal from an external clock generator is connected here. Refer to paragraph 3-5.

3-35. PRBS OUTPUT.

3-36. In DIVIDE and NORM, this signal corresponds to the output of the last shift register cell.

3-37. In MULTIPLY, this signal corresponds to the sum of the output of the last shift register cell and the data input.

3-38. ERROR OUTPUT.

3-39. There will be a pulse out of this output connector whenever the data input and the PRBS output are different. The signal is used in conjunction with the data synchronization provision to measure the errors generated by a communications channel or any device for processing digital data.

3-40. TRIGGER.

3-41. This output is a trigger pulse to allow synchronizing another instrument, such as an oscilloscope, to the PRBS pattern of the Model 1930A. The output is effective only in the NORM-PRBS mode and corresponds to the shift register state 000...001.

3-42. REGISTER RESET.

3-43. This control causes all cells in the shift register to reset to zero and remain at zero while the pushbutton is pressed. When the pushbutton is released, an internal circuit will detect the all-zero condition and load a one into the first shift register cell. This permits normal operation to resume.

3-44. OPERATING PROCEDURES.

3-45. It is not within the scope of this manual to describe the operation of the Model 1930A in all possible applica-

tions since this is dependent upon the auxiliary equipment being used in the application. This procedure will describe the operation of the instrument in each of it's basic functions, then describe it's use as one or more elements in a complete operating or testing system. Further information may be obtained from Application Notes available from Hewlett-Packard Sales/Service Offices.

3-46. The Model 1930A has three basic functions. They are as follows:

a. Data source.

b. Bit-error detector.

c. Cryptographic encoder/decoder.

NOTE

The Model 1930A can be used with a wide variety of auxiliary equipment. Greatest ease of operation and best results may be obtained when other HP 1900-series plug-ins are selected as auxiliary equipment. These units may be conveniently plugged into the 1900-series mainframe along with the Model 1930A. Refer to Table 3-2 for a list of such auxiliary equipment.

3-47. DATA SOURCE.

3-48. The MODEL 1930A may be used to generate binary words or to generate pseudo-random binory sequences (PRBS).

3-49. To operate the Model 1930A as a PRBS source, proceed as follows:

a. Connect equipment as shown in Figure 3-2.

b. Set Model 1930A controls as follows:

REGISTER LENGTH . . . . . as desired
PRBS/WORD . . . . . PRBS
MULTIPLY/NORM/DIVIDE . . . . . NORM
RZ/NRZ . . . . . refer to requirements of device under test.

3-50. To operate the Model 1930A as a binary word source proceed as follows:

a. Connect equipment as shown in Figure 3-2.

b. Set Model 1930A REGISTER LENGTH SWITCH to PGM.

c. Since a very limited number of words are available in front panel operation, it is recommended that this mode of operation be limited to programed operation. Refer to paragraph 3-70.

Table 3-2. Auxiliary Equipment for Use in Systems with Model 1930A

Use	Equipment
Clock Generator	HP 1905A Rate Generator HP 1906A Rate Generator
Data Source	HP 1925A Word Generator HP 1930A PRBS Generator HP 3722A Noise Generator
Delay	HP 1908A Delay Generator HP 1910A Delay Generator
Error Counter	HP 5245 Electronic Counter HP 5246 Electronic Counter HP 5248 Electronic Counter
Shaper	HP 1915A Variable Transition Time Output HP 1917A Variable Transition Output HP 1920A Fixed Transition Generator HP 1921A Fixed Rise and Fall Output Amplifier, Positive HP 1922A Fixed Rise and Fall Output Amplifier, Negative

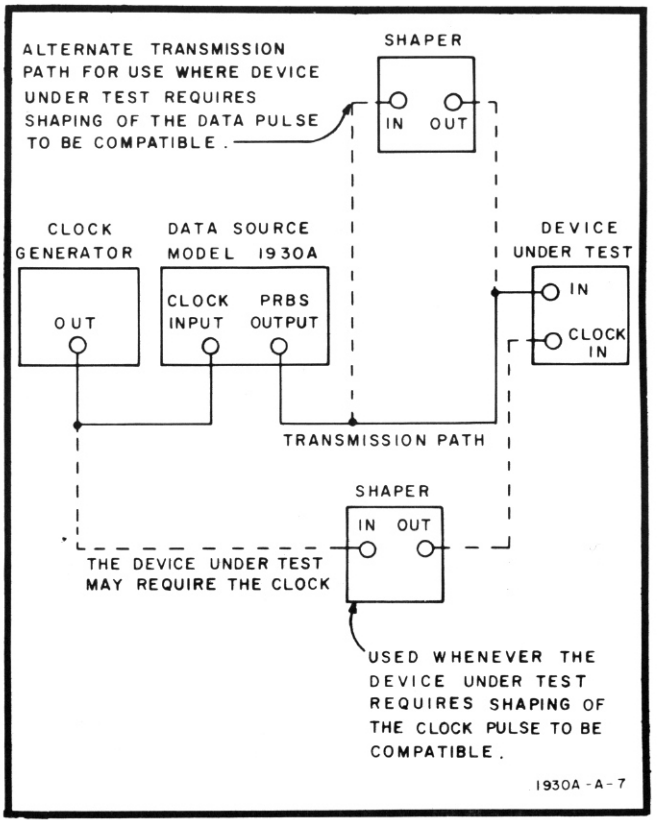


Figure 3-2. Data Source Operation.

d. Program WORD and MULTIPLY modes.

e. Refer to the requirements of the device under test and program RZ or NRZ as required.

f. There is a limitation to this mode of operation. Because the length of the word is determined by the last enabled shift register feedback tap, the last inserted bit must be a one. Additionally, as explained in Section IV, the method used to produce this mode of operation causes a trailing zero to appear at the end of each word. The total effect is to limit the last two bits of each word to 10. The word length will be N + 1 instead of N.

3-51. BIT-ERROR DETECTOR.

3-52. To operate the Model 1930A as a bit-error detector, proceed as follows:

a. Connect equipment as shown in Figure 3-3.

b. Set Model 1930A controls as follows:

REGISTER LENGTH . . . To match data generator
PRBS/WORD . . . . . To match data generator
MULTIPLY/NORM/DIVIDE . . . . . NORM

NOTE

The feedback structure or characteristic equation of the shift register in the data generator must be known. No knowledge of the data content of the digital sequence is required.

c. Press the DATA SYNC pushbutton and hold until DATA SYNC lamp lights.

d. Release the pushbutton. Error rate may now be read directly from the error counter.

e. If the error rate is greater than 1×10^{-4}, the data sync lamp will not light even through synchronization has been achieved. Determine instrument synchronization with the data input by observing error rate as measured by the counter. If the data is unsynchronized, the counter will read approximately one-half of the clock rate. For instance, if the clock rate is 100 kHz, a reading of 50 kHz on the counter will indicate an unsynchronized condition. If the counter reading is some value lower than 50 kHz caused by channel noise, synchronization is indicated.

f. The probability of achieving synchronization on the first attempt will be greater than one-half when the probability of a bit error is less than 3×10^{-2}.

3-53. ENCODER/DECODER.

3-54. ENCODER. To operate the Model 1930A as an cryptographic encoder, proceed as follows:

a. Connect equipment as shown in Figure 3-4.

b. Set Model 1930A front-panel controls as follows:

REGISTER LENGTH . . . . . Desired length
PRBS/WORD . . . . . PRBS
MULTIPLY/NORM/DIVIDE . . . . . DIVIDE
RZ/NRZ . . As required for data transmission link.

3-55. DECODER. To operate the Model 1930A as an cryptographic decoder, proceed as follows:

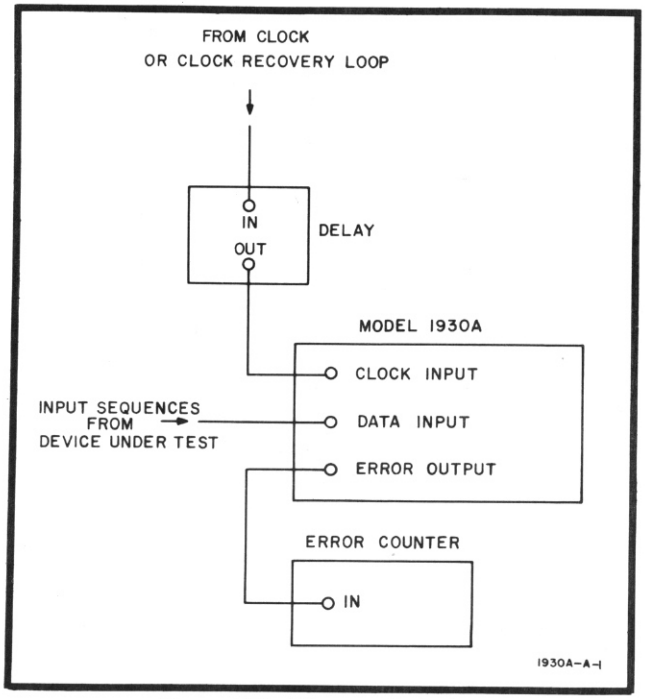


Figure 3-3. Bit-error Detector

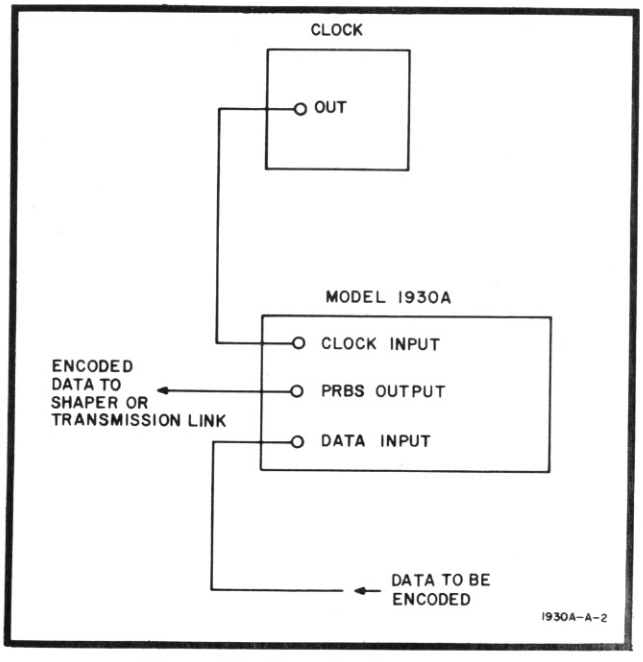


Figure 3-4. Encoder Operation.

a. Connect equipment as shown in Figure 3-5.

b. Set Model 1930A controls as follows:

REGISTER LENGTH . . . . . To match encoder
PRBS/WORD . . . . . PRBS
MULTIPLT/NORM/DIVIDE . . . . . MULTIPLY
RZ/NRZ . . As required for data transmission link.

c. Synchronization occurs automatically.

3-56. More complicated word and encode/decode sequences may be generated by connecting two or more Model 1930A's in series (see Figure 3-6). All front panel controls except REGISTER LENGTH on each unit are duplicated. REGISTER LENGTH switches must be set in combinations which have no common factors. Table 3-3 lists all such combinations for two units in series. The length of the resultant sequence will be the multiple of the individual sequences.

3-57. SYSTEM APPLICATIONS.

3-58. Figure 3-7 illustrates the Model 1930A in a complete system which demonstrates all three of it's basic functions.

3-59. CLOCK GENERATOR. This provides the basic timing and is essential in all applications (refer to paragraph 3-5).

3-60. INPUT DATA PROCESSOR. Used only when the DATA SOURCE functions as an cryptographic encoder. This represents the system which generates the data to be encoded.

3-61. DATA SOURCE. The sequences generated by this instrument must be compatible with the Model 1930A; that is, the shift registers must have the same characteristic equations. When used as a cryptographic encoder, it must be a Model 1930A.

3-62. SHAPER. Shaping may or may not be necessary. It assures that the pulses in the transmitted sequences are

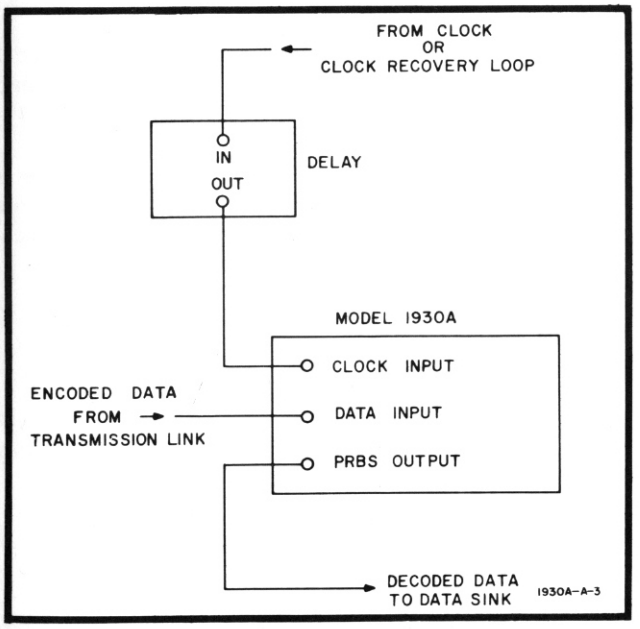


Figure 3-5. Decoder Operation.

Table 3-3. List of Integers N and M for which 2^N-1 and 2^M-1 have no Common Factors

N	M
3*	2
4	3
5*	2 3 4
6	5
7*	2 3 4 5 6
8	3 5 7
9	2 4 5 7 8
11*	2 3 4 5 6 7 8 9 10
12	5 7 11
13*	2 3 4 5 6 7 8 9 10 11
14	3 5 9 11 13
15	2 4 7 8 11 13 14
16	3 5 7 9 11 13 15
17*	2 3 4 5 6 7 8 9 10 11 12 13 14 14 16
18	5 7 11 13 17
19*	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
20	3 7 9 11 13 17

(*) Indicates that both N and 2^N-1 are prime integers

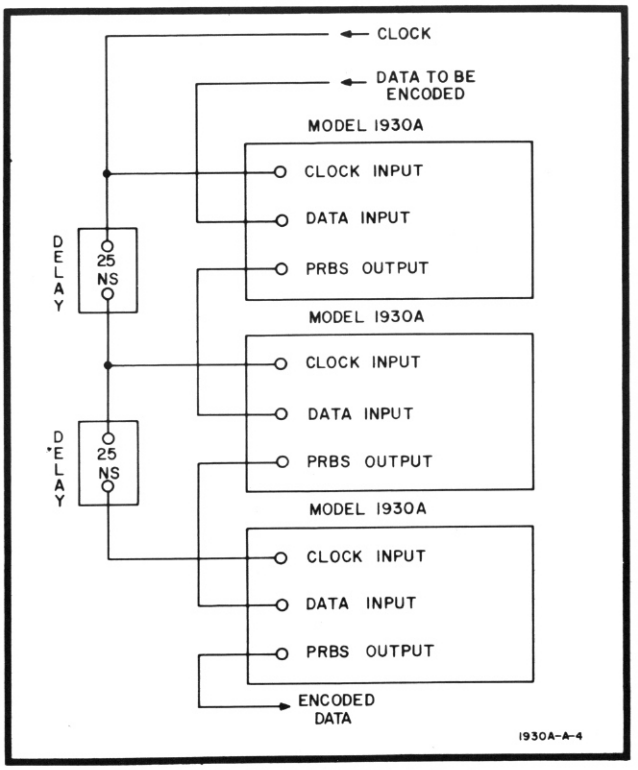


Figure 3-6. Model 1930As in Series.

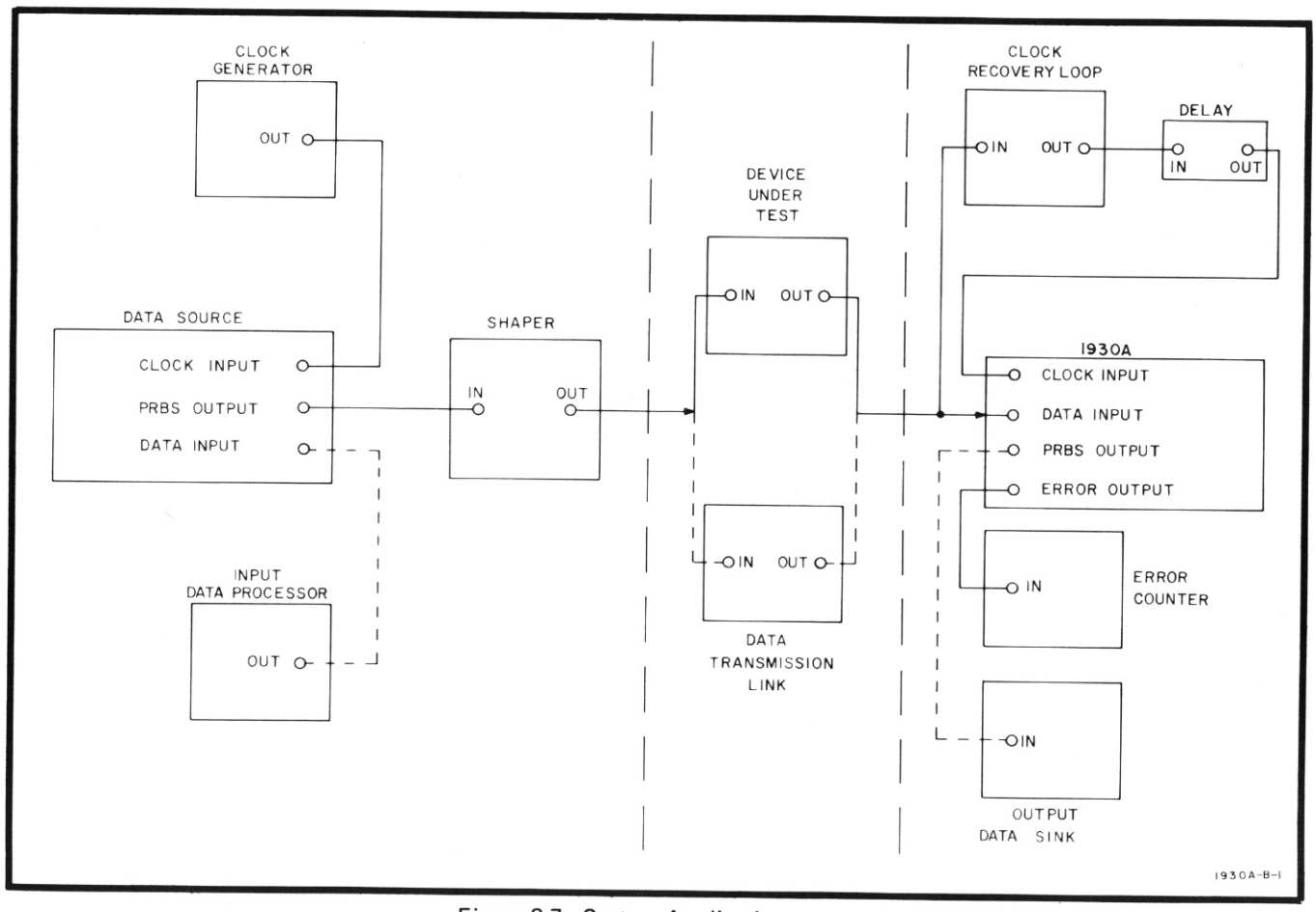


Figure 3-7. System Applications.

compatible with the transmission link or with the device under test.

3-63. DEVICE UNDER TEST. This assumes that the system is being used as a bit error detector. The device being tested may be a transmission line, a complete data link, modem, a shift register, or any number of other equipments which transmit and/or process digital information.

3-64. DATA TRANSMISSION LINK. Used to demonstrate the system in the encode/decode function. Examples are: A digital transmission line, telephone line, or radio link. Transmission (encoding) and reception (decoding) need not be a simultaneous process. The encoded data may be stored in a recorder or computer for later recovery and decoding.

3-65. CLOCK RECOVERY LOOP. The same clock frequency must be used to time the entire system. If the Model 1930A is remote from the DATA SOURCE, the clock must either be recovered from the data sequences or transmitted separately. If the Model 1930A is not remote from the DATA SOURCE, the clock may be connected directly from the clock generator.

3-66. DELAY. This element may or may not be necessary. For maximum wideband operation, the data input transitions should not become coincident with the risetime of the clock input. If the clock input occurs during the first 10 ns of the data input pulse, erratic operation will result. This condition may be prevented by delaying the clock input with a delay line or one of the units listed in Table 3-2.

3-67. MODEL 1930A. This block demonstrates the Model 1930A as a bit-error detector or as an cryptographic encoder/decoder.

3-68. OUTPUT DATA SINK. Used to demonstrate a system to accept and process the decoded data when the system is used in a cryptographic encode/decode application.

3-69. PROGRAMING INFORMATION.

3-70. REMOTE PROGRAMING.

3-71. The programing procedure which follows assumes that selection of the feedback taps has been made.

3-72. To program the Model 1930A to specific modes and feedback taps, proceed as follows:

a. Programing signals from DTL/TTL logic or switch closures must be applied to the rear panel connectors

(refer to Table 3-4) of the 1900-series mainframe and, in turn, to the program connector on the rear of the Model 1930A.

Table 3-4. 1900-series Mainframe Program Connectors

1900 Module Port	1900 Rear Panel Connector	1900 Internal Connector	1930A Rear Panel Connector
Left	J5	J9	P2
Left Center	J6	J10	P2
Right Center	J7	J11	P2
Right	J8	J12	P2

b. Figure 3-8 shows rear panel input connectors and internal mainframe connectors. For location of the module program connector see Figure 3-9. Table 3-5 provides the program connector interfacing necessary to program the Model 1930A.

3-73. SELECTION OF FEEDBACK TAPS.

3-74. When the register length switch is set to PGM, all the front panel controls will be transferred to the electronic programing inputs. The programing logic is listed in Table 3-6 and program specifications in Table 1-1. The functions are stated in positive logic. For example, to make $\overline{K2}$ true, then pin P2–2 ($\overline{K2}$) must be low or at ground potential. Similarly, for RESET to be false, pin P2–24 must be grounded.

3-75. In the programing mode, the feedback taps are not automatically chosen by the internal diode logic. Table 3-1 lists the feedback taps which are used in the front-panel mode (this table is also reproduced on the top panel of the Model 1930A). About 73,000 other maximal length pseudo-random sequences are possible. The feedback taps for these sequences may be found from tables of primitive irreducible polynomials over GF (2).

NOTE

These tables and other pertinent information may be found in:

a. Peterson, W. W., Error- correcting Codes. The MIT Press, Cambridge, Mass., 1961.

b. Golomb, Solomon W., Shift register Sequences. Holden-Day, INC., San Francisco, 1967.

c. Marsh, R. W., Tables of Irreducible Polynomials Over GF (2) Through Degree 19. NSA, Washington, D. C., 1957.

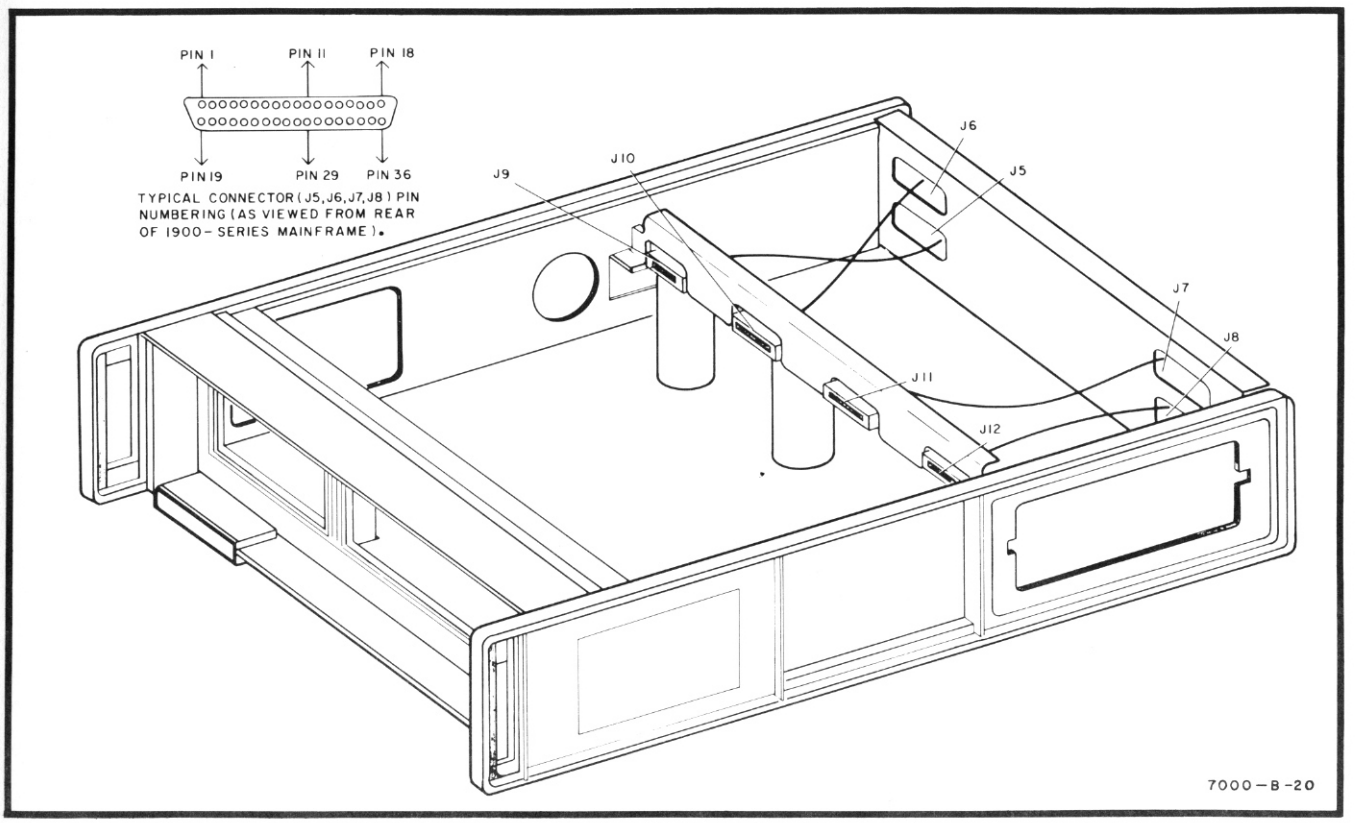


Figure 3-8. 1900-series Mainframe Connectors.

Table 3-5. Programing Inputs

To Program	Take Action Below	On Pin No.
Feedback Tap 1	ground	P2-1
Feedback Tap 2	ground	P2-2
Feedback Tap 3	ground	P2-3
.	.	.
.	.	.
.	.	.
Feedback Tap 20	ground	P2-20
Divide mode	ground	P2-21
Multiply mode	ground	P2-22
Normal mode	open	P2-21 & P2-22
RZ (return-to-zero)	ground	P2-23
NRZ (non-return-to-zero)	open	R2-23
Register reset	open momentarily	P2-24
External sync indicator	connect to external indicator	P2-24

Notes

1. Register reset, pin P2-24, must be grounded for normal operation.
2. Above instructions are for switch closure programing. If DTL logic is being used, substitute "logic 1" (+4V) for open and "logic 0" (OV) for ground.

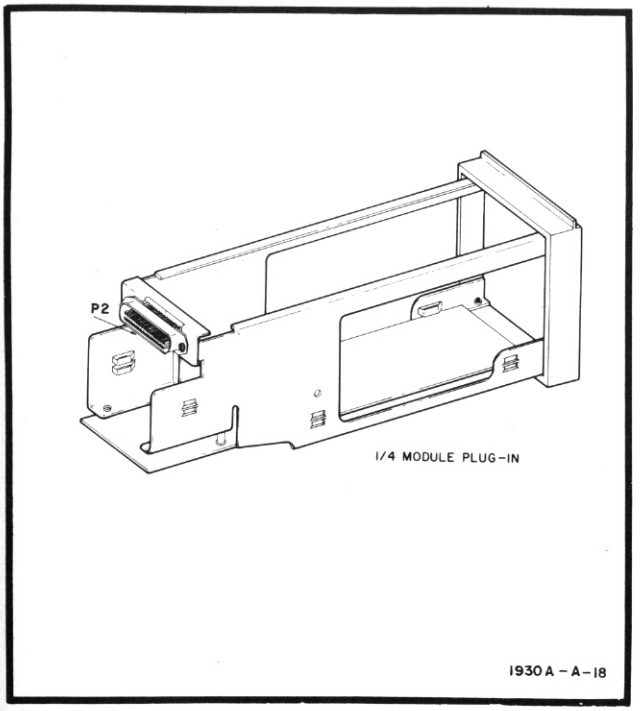


Figure 3-9. Location of Module Program Connectors.

3-76. Suppose a different 2047 ($2^{11}-1$) bit sequence was wanted other than the one listed in Table 3-1. Using Peterson's table of primitive irreducible polynomials as an example, the octal shorthand for many different 2047 bit sequences will be found under degree 11. If the 5221 polynominal is chosen, it will reduce to the binary equivalent:

(5)	(2)	(2)	(1)
101	010	010	001

Counting from the left-hand side indicates that the proper feedback taps are: 0, 2, 4, 7 and 11. Note that the zero tap in the Model 1930A is always closed. The inverse sequence can be generated by counting from the right-hand side to determine the feedback taps. They are:

0, 4, 7, 9 and 11.

3-77. If one or more sequences are to be used repeatedly in the PGM mode, they may be operated from one logic line by using diode logic from the command line to the appropriate feedback taps for the command.

3-78. ADDITIONAL APPLICATIONS.

3-79. Switch A1S1 has been added to input/output board A1 as a convenience to Model 1930A users who wish to adapt the instrument for use in convolutional encoding systems. The switch permits the output to be taken from the last shift register cell, as in the DIVIDE mode, with the shift register in MULTIPLY mode. For all normal operations as described in this manual, A1S1 remains in it's open position (direction of arrow).

Table 3-6. Programing Logic

Pin	Logic
P2–1	$\overline{K1}$
P2–2	$\overline{K2}$
P2–3	$\overline{K3}$
.	.
.	.
.	.
P2–20	$\overline{K20}$
P2–21	$\overline{DIVIDE}$
P2–22	$\overline{MULTIPLY}$
P2–23	NRZ
P2–24	RESET
P2–30	SYNC (DTL Output, –.6V to +4.5V)
P2- 36	GROUND

Positive Logic: High voltage or open is true

Low voltage or short is false

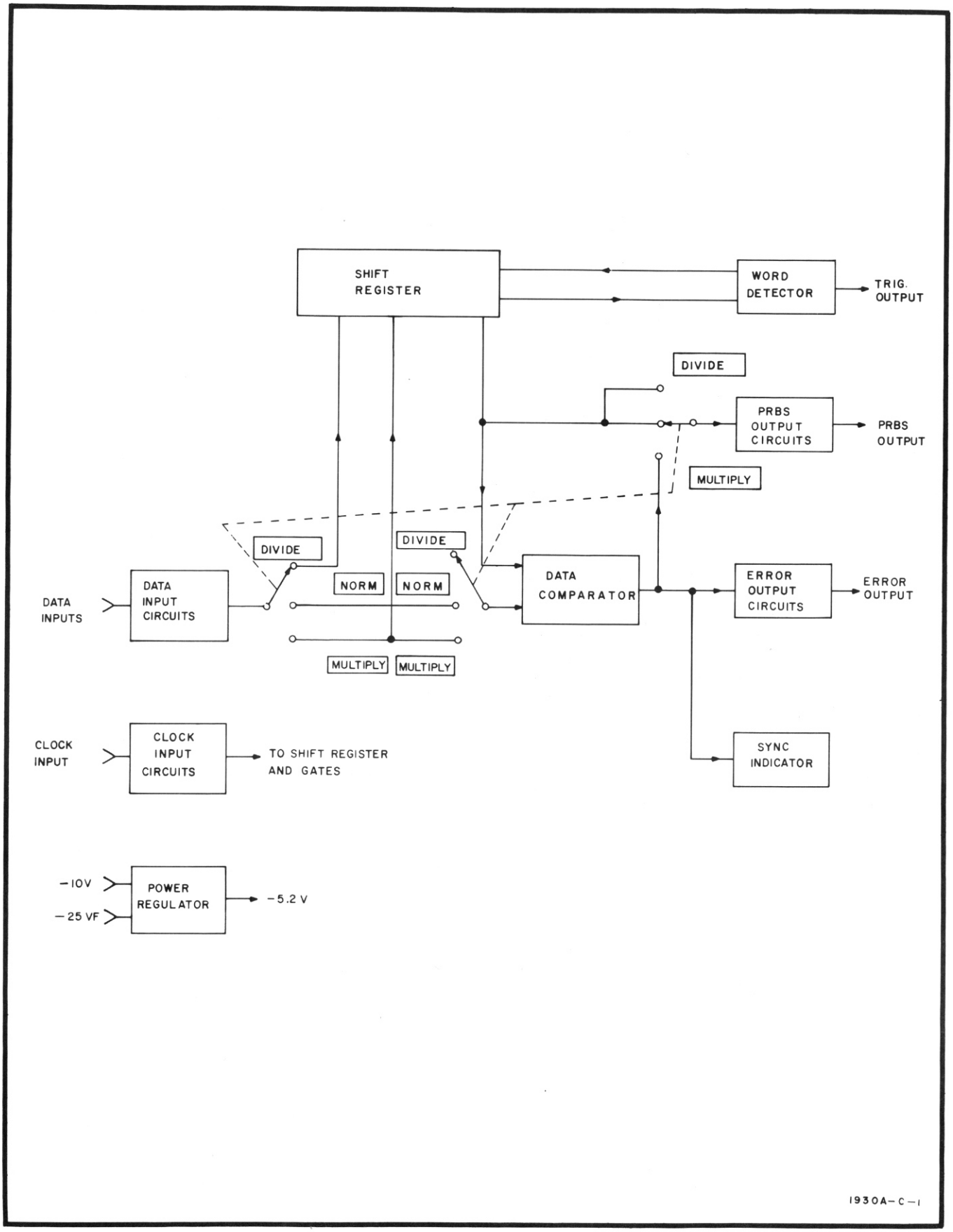


Figure 4-1. Block Diagram

SECTION IV

PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section provides circuit theory analysis of the Model 1930A. Circuit theory is first covered by a detailed discussion of general theory. The circuit details are then explained and referenced to the schematic diagrams. The schematics are located in Section VIII. Each schematic can be unfolded for reference while reading the applicable text.

4-3. The Model 1930A is one of a family of discrete digital data generators. Because it has both inputs and outputs, it has the ability to process digital data as well as to generate it. The instrument may be remotely controlled by electronic programing.

4-4. BLOCK DIAGRAM.

4-5. The Model 1930A is basically a shift register with input, control, and output circuits as shown in the block diagram (Figure 4-1). The control circuits (logic gates) are represented in the block diagram by the MULTIPLY/NORM/DIVIDE switch. The actual control circuits in the instrument are actuated by the front-panel MULTIPLY/NORM/DIVIDE switch.

4-6. The purpose of the clock and data buffers is to assure that the dc levels of input signals are compatible with the circuits of the shift register and control circuits.

4-7. Pulses from an external clock generator are applied to CLOCK INPUT and through the clock buffer to each shift register cell and the control gates. Data is shifted in and out of the instrument in step with the clock pulses.

4-8. In NORM, the shift register will generate pseudo-random binary sequences (PRBS). The sequences are directed through the PRBS output circuits to PRBS OUTPUT jack. The instrument performs as a data generator or transmitter.

4-9. In NORM, the Model 1930A may also be used to receive data and to function as a bit-error detector. The shift register will generate PRBS as before. If another instrument is generating the exact same sequence, the remote sequence can be applied to DATA INPUT. The output of the shift register and the output of the data input circuits are directed to the inputs of the data comparator where a a bit-by-bit comparison takes place. As long as the two sequences are identical, there is no output from the data comparator. If the transmission medium between the remote generator and the DATA INPUT of the Model 1930A should introduce an error (usually a noise pulse), an error pulse will be delivered to ERROR OUTPUT. The error pulses may be counted to determine the error rate of the transmission medium.

4-10. In DIVIDE, data is brought through the data buffer and into the shift register where it is combined with the sequence generated there.

4-11. Mathematically, the result of this combination is that the input data is divided by the characteristic equation of the shift register.

4-12. The divide configuration is useful in the field of cryptography. The data stream which has been combined with the self generated sequence in the shift register has in effect, been scrambled or encoded. The encoded data is directed through the PRBS output circuits to PRBS OUTPUT.

4-13. In MULTIPLY, input data is again combined with the sequence in the shift register. The output of the shift register is directed through the data comparator, then through the PRBS output circuits to PRBS OUTPUT.

4-14. Mathematically, this operation multiplies the input data by the characteristic equation of the shift register.

4-15. The multiply configuration is also useful in cryptography. If the input data has been encoded in another Model 1930A, it will be decoded in a Model 1930A in the multiply configuration.

4-16. The zero detector samples all shift register cells. If all cells except the first (output) cell contain a zero, the word detector will function as follows:

If the first cell contains a one, a pulse will be delivered to TRIGGER OUTPUT. The 000 . . . 001 condition occurs once during each PRBS cycle and the resultant output pulse can be used to trigger an oscilloscope or other external instrument. If the first cell contains a zero (on undesirable condition), the word detector will deliver a signal back to the shift register, restarting its operation.

4-17. The sync indicator monitors the error pulses to determine if the external sequence at DATA INPUT is in synchronization with the self generated sequence in the shift register. A low incidence of error pulses indicates synchronization and the sync indicator circuits will cause the SYNC lamp on the front panel to light.

4-18. The output circuits, PRBS and ERROR, each contain gates which determine whether the output format

will be NRZ (nonreturn to zero) or RZ (return to zero). They also contain amplifier circuits whose chief purpose is impedence matching.

4-19. GENERAL THEORY.

4-20. The following paragraphs explain the operation of the Model 1930A. Necessary basic information is given followed by detailed explanations using illustrations and charts to demonstrate circuit logic.

4-21. BASIC INFORMATION.

4-22. The integrated circuits are of the emitter-coupled logic design. The typical circuit uses a differential amplifier as the input circuit with an internal bias reference and emitter-follower outputs to shift the dc level.

4-23. The Model 1930A is basically a digital shift register. The shift register is constructed of D-type flip-flops, NOR gates and exclusive NOR gates. These three elements and their truth tables are shown in Figure 4-2.

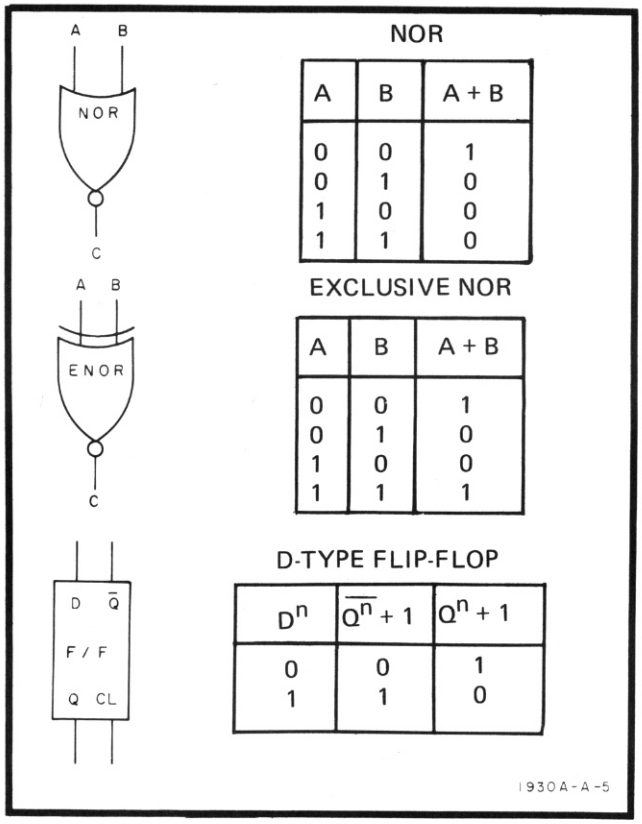


Figure 4-2. Basic Shift Register Elements

4-24. The NOR gate output is only true (−0.7 volt) when both inputs are false (−1.5 volts). The exclusive NOR output is true when both inputs are false or when both inputs are true; that is, the output is true whenever the inputs are the same.

4-25. The storage cells used in the Model 1930A shift register are all type D master-slave flip-flops. The Q output, after a clock pulse, will be whatever was on the D input just before the clock pulse. The $\overline{Q}$ (NOT Q) output will be the reciprocal of whatever was on the D input before the clock pulse.

4-26. WORD GENERATION.

4-27. Figure 4-3 shows how the elements discussed above can be combined to form a feedback shift register for generating digital words and sequences. If the feedback taps ($\overline{K3}$ etc) are not programmed (A input at logic 1) the C outputs of the NOR gates are held at logic 0. When a feedback tap is programmed (A input at logic 0) the C output will be the reciprocal of whatever is on the feedback line. The output of the ENOR gates will be logic 0 if the A and B inputs are different and logic 1 if they are the same. This results in the D input to any cell being the exclusive OR combination of F/F1 - Q1 and ENOR - A. The output of each shift register cell can be expressed as follows:

$$D3 = \overline{\overline{1} \oplus NOR3}$$

$$NOR3 = \overline{\overline{K3} + \overline{Q1}}$$

$$D3 = \overline{\overline{1} \oplus \overline{\overline{K3} + \overline{Q1}}}$$

$$= \overline{\overline{1} \oplus (K3 \cdot Q1)}$$

$$= 0 \oplus (K3 \cdot Q1)$$

$$= K3 \cdot Q1$$

$$Q3 = \overline{(K3 \cdot Q1)}D \text{ where D}$$

$$= \text{1 bit delay operator}$$

Similarly: $Q2 = [Q3 \oplus (K1 \cdot Q1)]\,D$

and $Q1 = [Q2 \oplus (K1 \cdot Q1)]\,D$

4-28. Suppose $\overline{K3}$ is programmed (logic 0) and the outputs of the 3 cells are arbitrarily assigned values as shown in line 1 of the word table in Figure 4-3. $\overline{K3}$ having been enabled, logic 0 on the feedback line is inverted by NOR 3. Both inputs to ENOR3 being logic 1, its output and D3 are logic 1. Since NOR1 and NOR2 are disabled (not programmed), D2 and D1 are both logic 0. After the next clock pulse, the reciprocal of the D inputs transfer to the $\overline{Q}$ outputs establishing the condition shown in line 2 of the word table.

4-29. The $\overline{Q1}$ output and the feedback line are now logic 1. The NOR outputs are 000. The ENOR outputs are 010. After the next clock pulse the reciprocals of these values are on the $\overline{Q}$ outputs of the cells.

4-30. $\overline{Q1}$ is again logic 1. The NOR outputs are 000. The ENOR outputs are 001. After another clock pulse the $\overline{Q}$ outputs are 110 as shown in line 4 of the word table. This is the same as line 1. The sequence will endlessly repeat itself until the conditions of the shift register are changed. The word at the output of the inverter will be 100 as shown in the output column of the word table.

4-31. When K3=0 and K2=K1=1 as described in the above paragraphs, the mathematical expressions are:

$$Q1 = Q2 \cdot D$$

$$Q2 = Q3 \cdot D$$

$$Q3 = Q1 \cdot D$$

4-32. SEQUENCE GENERATION.

4-33. Suppose $\overline{K3}$ and $\overline{K2}$ are programmed (logic 0). A longer and more interesting result is now obtained. The values shown in line 1 of the Sequence Table in Figure 4-3 are arbitrarily assigned.

4-34. NOR3 and NOR2 are activated (programmed) and logic 0 on $\overline{Q1}$ is inverted by the two NORs. The outputs of the NOR gates are 110. The outputs of the ENORs are 110. After a clock pulse, the $\overline{Q}$ outputs of the cells are 001 as shown in line 2 of the sequence table. If a node by node check of the circuit is made after each clock pulse the conditions shown in lines 3 through 8 of the sequence can be verified. Line 8 is the same as line 1. The shift register will endlessly generate this sequence until conditions are changed.

4-35. After passing through the inverter, the word generated is 1011100. This is a pseudo - random sequence of maximal length (2^N - 1) which in this case is 2^3 - 1 or 7 bits long. N=3 because there are 3 shift register cells involved.

4-36. When $\overline{K3}$=$\overline{K2}$=0 and $\overline{K1}$=1 as described above, the mathematical expressions are:

$$Q1 = Q2 \cdot D$$

$$Q2 = (Q1 \oplus Q3)\, D$$

$$Q3 = Q1 \cdot D$$

hence: $Q1 = [Q1 \oplus (Q1 \cdot D)]\, D^2$

or $Q1(1 + D^2 + D^3) = 0$

characteristic equation $= 1 + D^2 + D^3$

general characteristic equation

$= 1 + K1D^1 + K2D^2 + K3D^3 \cdots K20D^{20}$

4-37. Word generation and sequence generation are examples of the shift register operating in the feedback configuration. Mathematically, feedback looks like division, and while the basic feedback configuration is called NORM on the front panel, one form of the feedback configuration is called DIVIDE on the front panel.

4-38. FEED-FORWARD.

4-39. Mathematically, feed-forward looks like multiplication, so the feed-forward mode is called MULTIPLY on the front panel. A special case of the multiply operation is shown in Figure 4-4.

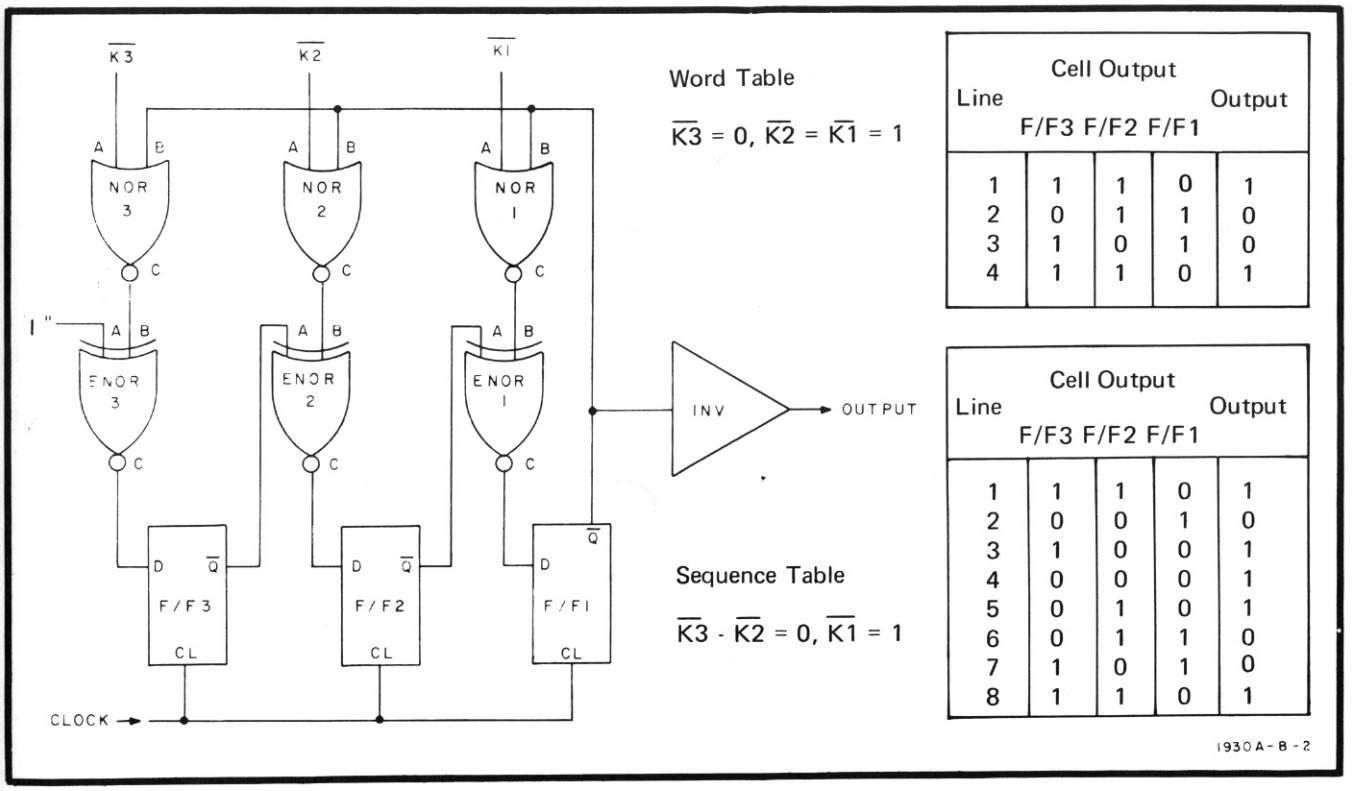


Figure 4-3. Feedback shift Register for Generating Digital Words and Sequences

4-40. The basic operation shown in Figure 4-4 is useful to troubleshoot the shift register of the Model 1930A. The feedline F is driven by a circuit (here represented by a simple OR circuit) that detects all zeros in the shift register. If the initial condition is all zero, the condition shown in line 1 of the feed-forward table will be established and the output of the all zero detector will be logic 0. If $\overline{K3}$ and $\overline{K2}$ are logic 0 and $\overline{K1}$ is logic 1, using the same logic as shown for feedback operation (word and sequence generators), then logic 1 will be loaded into the $\overline{Q}$ outputs of F/F3 and F/F2 and logic 0 into F/F1 and the condition shown in line 2 of the table will be setup.

4-41. The output of the all-zero detector now goes to logic 1 disabling the NOR circuits. The next clock pulse will advance both 1s one position establishing the condition shown in line 3 of the table. A second clock pulse establishes the condition down in the line 4, and a third clock pulse establishes the condition shown in line 5 of the table, which is the same as the original condition. The all zero detector will again function and the entire procedure will repeat, continuously generating the word 0110. The word length is N + 1 which in this case is 3 + 1 or 4 bits long. N=3 because there are three shift register cells involved.

4-42. Because the word length is determined by the last activated feedback tap, in this case $\overline{K3}$, the next to last bit in each word generated in this configuration is always logic 1. Because the shift register always returns to the all zero condition before the sequence is repeated, the last bit is always logic 0.

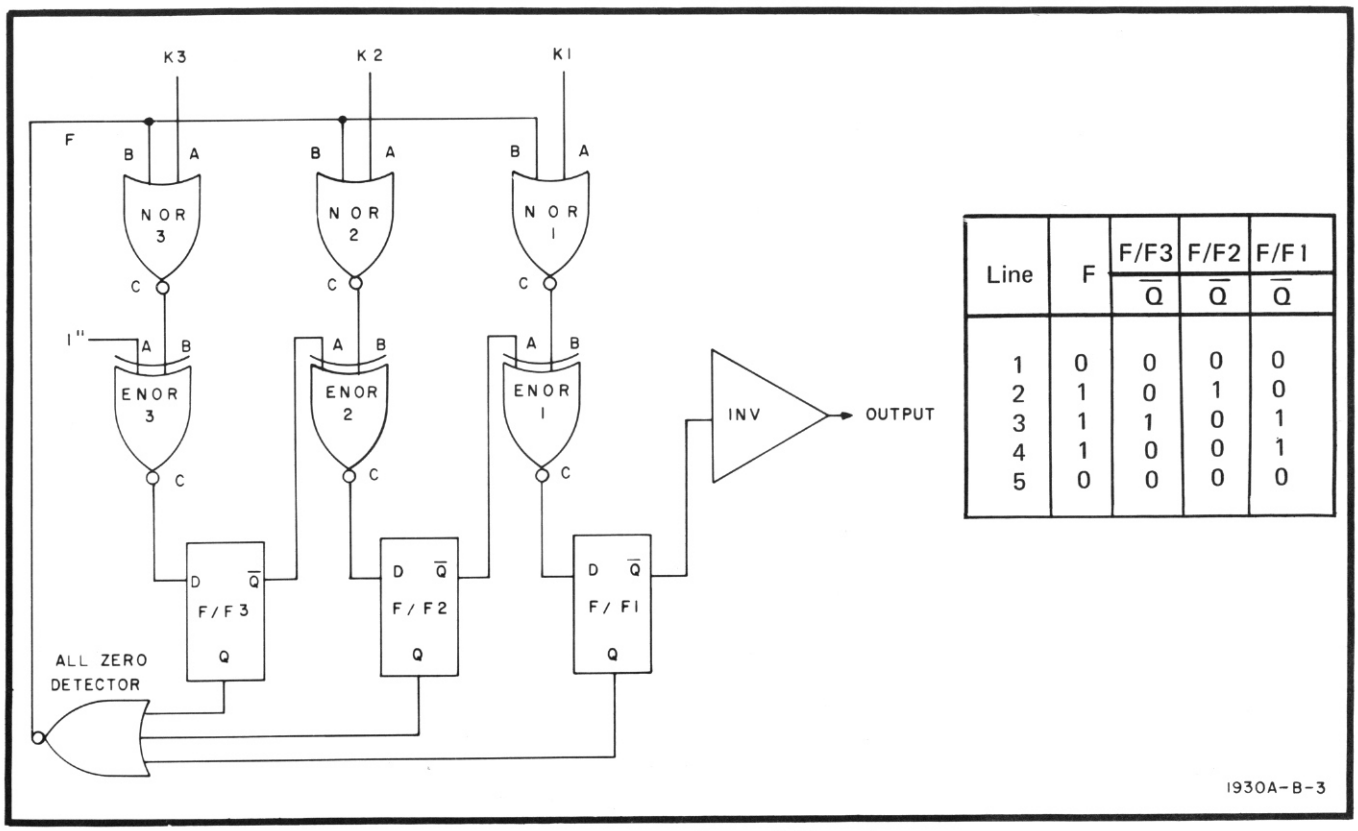
4-43. This configuration provides a very convenient method of checking the operation of all flip-flops and gates in the shift register.

4-44. SYNCHRONIZATION.

4-45. Paragraphs 4-38 through 4-43 described a special case of multiply operation where the feed-forward line was driven by the all zero detector. A more useful function of the feed-forward configuration is that of synchronizing two PRBS generators. This is accomplished by driving the feed-forward line of one unit by the output of another.

4-46. The MULTIPLY function of the MULTIPLY/NORM/DIVIDE switch is duplicated by the SYNC pushbutton switch. It is placed on the front panel to make synchronization more covenient.

4-47. Figure 4-5 shows the combined circuits of Figures 4-3 and 4-4 in simplified form. Unit 1 represents a Model 1930A (or any other compatible PRBS generator) in the feedback (NORM) configuration. Unit 2 represents a Model 1930A in its feed-forward (multiply) configuration. The simplified representation illustrates that the feedline in both units are driven by the same source (output of Unit 1 F/F1). To make the units compatible with Figures 4-3 and 4-4, treat the inputs of each F/F block as if it were an exclusive NOR circuit.



Line	F	F/F3 $\overline{Q}$	F/F2 $\overline{Q}$	F/F1 $\overline{Q}$
1	0	0	0	0
2	1	0	1	0
3	1	1	0	1
4	1	0	0	1
5	0	0	0	0

Figure 4-4. Multiply (Feedforward) Operation

4-48. The values shown in line 1 of the synchronization table in Figure 4-5 were arbitrarily assigned and exclusive NOR logic then applied to obtain the values shown in lines 2 through 8. Unit 1 is generating the sequence 1011100 exactly as shown in Figure 4-3 and, beginning at line 4, Unit 2 is generating the same word in unison with Unit 1. Thus, synchronization has been achieved.

4-49. Both units must be timed with the same clock frequency, so if Unit 2 is returned to NORMAL operation after synchronization has been achieved both units will continue to generate the same word in unison.

4-50. The self-generated sequence from Unit 2 and the sequence from Unit 1 are presented to an error detecting circuit in Unit 2 for a bit-by-bit comparison. If the transmission medium between the output of Unit 1 and the input of Unit 2 should introduce an error (usually a noise pulse) the error detecting circuit will generate an error pulse.

4-51. ENCODE/DECODE OPERATION. If a Model 1930A is operated in the divide mode and a data stream is introduced into it's DATA INPUT terminal, the PRBS output will be a data stream entirely different from either the data being introduced or it's own internally generated sequence. Further, if the PRBS output is introduced into the DATA INPUT of a second Model 1930A operated in it's multiply mode, the PRBS OUTPUT of the second unit will be a reproduction of data introduced into the first unit. There is one restriction to this operation; the feedback structure must be the same in both units. More specifically, the characteristic equations of the shift registers must be identical.

4-52. Such a set-up is shown in Figure 4-6. The output from the transmitter will be:

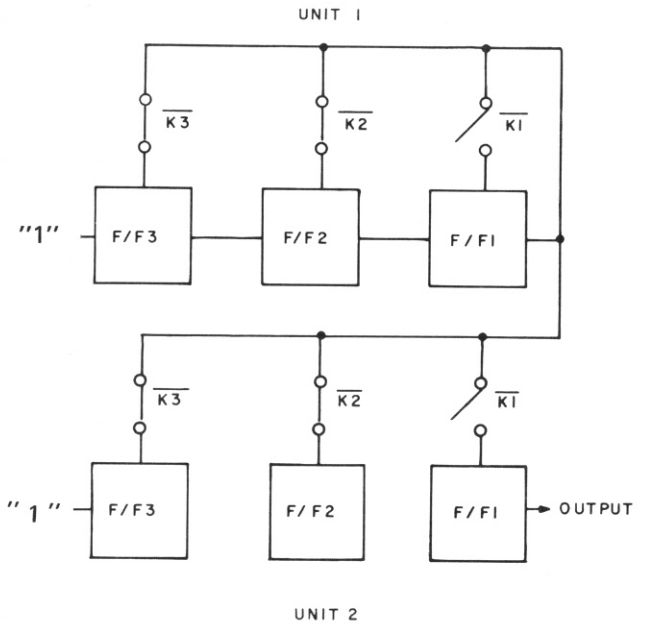
$$\emptyset 1 = \frac{D^1}{1 + D^2 + D^3}$$

where D = 1 bit delay operator

The output from the receiver will be:

$$\emptyset 2 = \frac{D1}{1 + D^2 + D3} \quad 1 + D^2 + D^3$$

$$= D1$$



Synchronization Table

All cells in unit 2 are same as in Unit 1.

Line	Unit 1			Unit 2		
	F/F3	F/F2	F/F1	F/F3	F/F2	F/F1
1	1	1	0	0	0	1
2	0	0	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	0	0
5	0	0	1	0	0	1
6	1	0	1	1	0	1
7	1	1	1	1	1	1
8	1	1	0	1	1	0
9	0	0	0	0	0	0

1930A-A-14

Figure 4-5. Synchronization

4-53. A bit-by-bit operation of the system is shown in the table in Figure 4-6. The outputs of the shift register cells have been arbitrarily selected as shown in line 1 of the table. The input word 1001101 is being introduced to DATA INPUT as shown in the IN column lines 2 through 9. Exclusive OR logic is applied to each input to obtain the shift register conditions shown in lines 2 through 9. Note that after a delay of one bit, the OUT column is identical to the IN column.

4-54. SHIFT REGISTER CONTROL. (Figure 4-7.)

4-55. All control (except feedback taps) of the shift register is accomplished in the input circuitry of F/F2 and F/F1. Since F/F20 through F/F4 are identical to F/F3 they are omitted from Figure 4-7 in order to simplify the diagram.

4-56. The various gates in Figure 4-7 function as follows:

a. Feedback gates 1 through 20 (1 through 3 shown) serve to combine data from selected feedback taps with data in the shift register.

b. The data steering gate, on command from the front-panel controls or from program controls, directs the data buffer amplifier to either the divide gate or to the data comparator. The data steering gate also provides enabling signals to the divide gate and to the multiply gate.

c. The multiply enable gate, on command from front-panel controls or from program controls, provides enabling signals to the multiply gate.

d. The multiply gate selects data either from F/F2 or from the data steering gate and directs it to F/F1.

e. The output gate selects data either from F/FA or from F/FB and directs it to the PRBS output circuits.

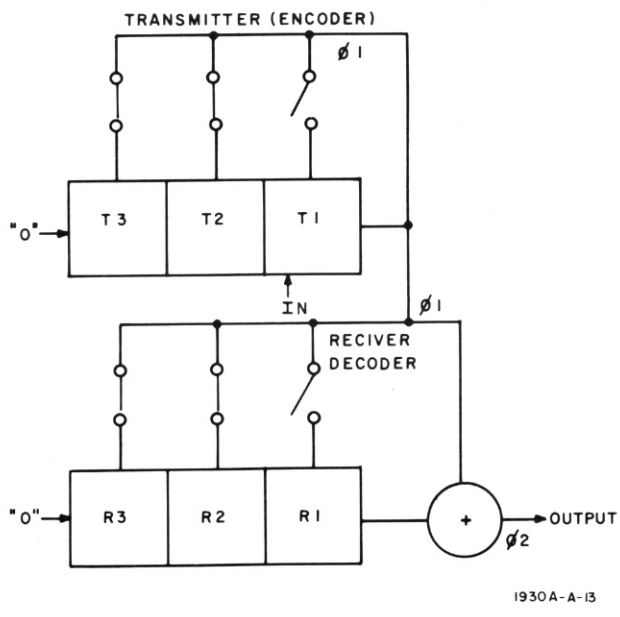
4-57. The discussions which follow assume that two or more of the feedback taps are activated and the shift register is generating a PRBS as described in Paragraphs 4-32 through 4-37.

4-58. NORMAL OPERATION. The NORM configuration is the basic feedback configuration. In NORM, the Model 1930A generates pseudo-random binary sequences which are directed to PRBS OUTPUT. It also compares this internally generated sequence with an externally generated sequence at the DATA INPUT terminal and causes a pulse to appear at ERROR OUTPUT when there is an error in the external sequence.

4-59. In NORM, the data steering gate enables the divide gate. The divide gate then permits the data in the shift register to pass from F/F3 to F/F2. The data from the data buffer amplifier will be directed to the data comparator.

4-60. The multiply enable gate enables the multiply gate to permit the data from F/F2 to pass to F/F1. F/F1 and F/FA are identical; F/F1 is used to drive the feedline and F/FA is used to drive the output circuits.

4-61. The output gate permits the output of F/FA to be connected to the output circuits and passed to PRBS OUTPUT.



Line	IN	Transmitter T3	T2	T1	Receiver R3	R2	R1	Ø2
1		1	1	1	1	1	1	
2	1	1	0	0	1	0	1	0
3	0	0	1	0	0	1	0	1
4	0	0	0	1	0	0	1	0
5	1	1	1	1	1	1	0	0
6	1	1	0	0	1	0	1	1
7	0	0	1	0	0	1	0	1
8	1	0	0	0	0	0	1	0
9	1	0	0	1	0	0	0	1

Figure 4-6. Encode/decode Operation

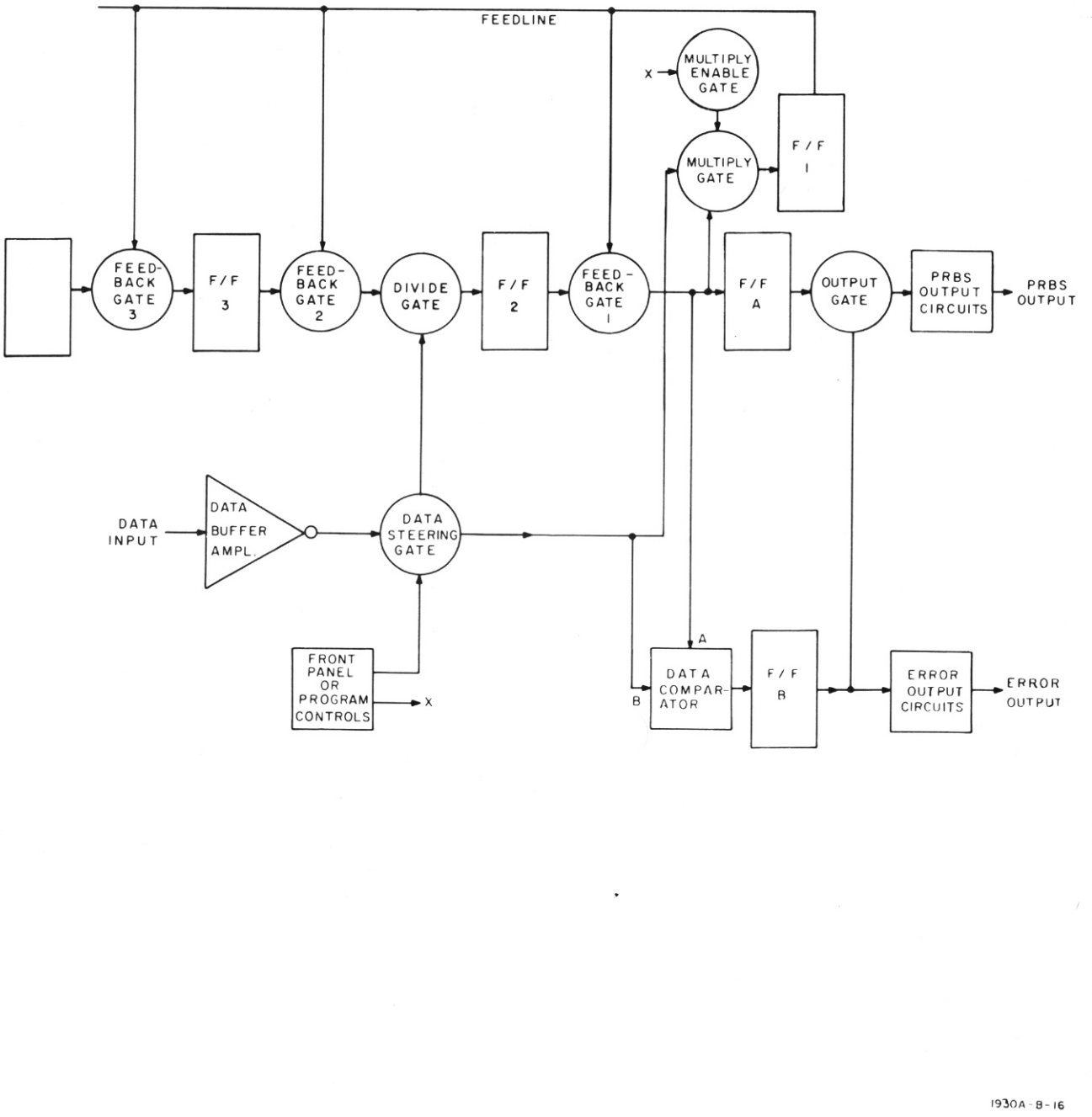


Figure 4-7. Shift Register Control

4-62. The sequence from DATA INPUT is present at the B input of the data comparator and the internally generated sequence from the shift register is at the A input. As long as the two inputs are equal there will be no output at ERROR OUTPUT. If an error occurs in the input data, the A and B inputs to the data comparator will be different and there will be a pulse at ERROR OUTPUT.

4-63. DIVIDE OPERATION. In DIVIDE, the data steering gate will direct the data from the date buffer amplifier to the divide gate. The data will be added to the self generated sequence in the shift register.

4-64. The multiply gate will direct data from F/F2 to F/F1 as before.

4-65. The output gate will direct the output of F/FA into the output circuits. The data at PRBS output will be the combination of the externally generated input data and the internally generated sequence.

4-66. MULTIPLY OPERATION. In MULTIPLY the data steering gate will direct the input data to the B input of the data comparator and to the multiply gate.

4-67. The multiply enable gate will direct the multiply gate to disconnect F/F1 from F/F2. The multiply gate will direct the input data to F/F1. The output of F/F1 still drives the feedline. Instead of data from the shift register being feed back to the register, the data from DATA INPUT is feed forward in the register.

4-68. The output gate connects the output of F/FB to the PRBS output circuits. PRBS OUTPUT will be the combination of the self generated sequence from the shift register and the externally generated sequence from DATA INPUT.

4-69. CIRCUIT DETAILS.

4-70. The following paragraphs provide a detailed discussion of Model 1930A circuits. The discussions are referenced to the schematics in Section VIII.

4-71. POWER SUPPLY REGULATOR. (See Schematic 2.)

4-72. The power supply regulator, consisting of A5Q1, A1Q1, A1Q3, A1Q5, and associated circuitry is a series-type regulator. It filters and reduces the −10V supplied by the mainframe. In addition, it protects the −10V power supply (mainframe) by limiting the amount of current that may be drawn.

4-73. A1VR1 and A1CR1 establish the voltage on the base of A1Q1. When A1Q1 conducts, it supplies base current to A5Q1. The collector to emitter voltage drop across series regulator A5Q1 determines the output voltage from the regulator circuit.

4-74. Suppose the −10-volt supply is going more negative. This change on the emitter of A5Q1 causes its collector-emitter current to increase. The increased current produces a more negative output voltage. This change is applied to the emitter of A1Q1, reducing the collector-emitter current and, consequently, A1Q1 supplies less emitter-base current to A5Q1. The reduction of A5Q1's emitter-base current reduces its emitter-collector current thereby causing the output voltage to go more positive, reducing the change caused by the input voltage.

4-75. Normally, current limiter A1Q2 and A1Q3 are cut-off. Should the output current exceed 1.8 amperes the voltage drop across A1R1 will cause A1Q2 to conduct. With A1Q2 conducting, the voltage across A1R5 rises, causing A1Q3 to conduct. The conduction of A1Q3 causes it's collector voltage to fall to such a low value that A1VR1 ceases conduction. With A1VR1 cut-off A1Q3 controls the base bias on A1Q1, reducing the emitter-base current. Because A1Q1 is supplying less current to the base of A5Q1, collector-emitter current of A5Q1 is reduced to maintain a constant current of 1.8 amperes.

4-76. When the overload is removed, A1Q2 will cut-off. The voltage across A1VR1 and A1CR1 will rise until A1VR1 conducts and normal voltage regulation will resume.

4-77. INPUT BUFFER AMPLIFIERS.

4-78. CLOCK BUFFER AMPLIFIER. The clock amplifier consists of A1Q4, A1Q6, A1Q7 and A1Q8. It shares voltage-source A1Q5 with the data amplifier.

4-79. A1Q4, A1Q6, and associated components form a pulse amplifier with a threshold of 0.3 volt. The threshold is established by resistive divider A1R15 and A1R16. A1R9 controls the base bias on A1Q5 and thereby the collector voltage supplied to A1Q4 and A1Q6. By establishing the bias on A1Q7 (voltage drop across A1R11), A1R9 varies the dc level of the emitter of A1Q7. This adjustment compensates for small differences in the threshold voltages of the shift register flip-flops.

4-80. Voltage divider A1R15/A1R16 biases A1Q6 off when the clock input is zero. On application of a positive pulse to CLOCK INPUT, A1Q4 turns off and A1Q6 turns on. This creates a negative signal at the collector of A1Q4.

4-81. The inverted pulse produced at the collector of A1Q4 is applied to the bases of complementary emitter followers A1Q7/A1Q8. The output at the emitters is delivered to four different places. Resistors A1R22, A1R23 and A1R24 serve to match the twisted pair transmission lines used to distribute the clock pulses to boards A2 and A3.

4-82. DATA BUFFER AMPLIFIER. The operation of the data amplifier, A1Q9/A1Q10/A1Q11, is identical to that of the clock amplifier, except that it's output is delivered through an ordinary emitter follower (A1Q11) instead of a complementary emitter follower.

4-83. DATA STEERING GATE.

4-84. The output from data emitter follower A1Q11 is distributed through the data steering gate which consists of OR gate A2U14. When the inputs to the OR gate are gate A1U1B. Distribution depends on the position of the front-panel MULTIPLY/NORM/DIVIDE switch.

4-85. In NORM and MULTIPLY, logic 1 on the $\overline{DIV}$ line disables A1U1A holding the $\overline{ID}$ line to logic 1 and the ID line to logic 0. Logic 1 on the $\overline{DIV}$ line is inverted by A1U2A enabling A1U1B and permitting data on the I line to the pass to the $\overline{IM}$ line.

4-86. In divide, logic 0 on the $\overline{DIV}$ enables A1U1A permitting data on the $\overline{I}$ line to pass to the $\overline{ID}$ line and to pass inverted to the ID line. Logic 0 on the $\overline{DIV}$ is inverted by A1U2A disabling A1U1B and holding the $\overline{IM}$ line to logic 1.

4-87. DIVIDE GATE. (Schematic 4.)

4-88. The divide gate, consisting of A2U21A, A2U21B, A2U21C and A2U22A, serves to add the feedback function and the output of A2U8 and uses the combination to drive the input of A2U9A. This is the same function performed by the exclusive NOR gates between the other shift register cells (Q20-Q3). The divide gate is more complicated because, in divide, it must also add the data input into the data stream.

4-89. In NORM and MULTIPLY, logic 1 on the $\overline{ID}$ line disables A2U21C and A2U22A. Logic 0 on the ID line enables A2U21A and A2U21B permitting data from A2U8 and feedback tap 2 (G2) to be combined at the D1 input of A2U9. These outputs can be expressed as follows:

A2U21A output: $Q3 \cdot \overline{ID} \cdot \overline{(F + K2)}$

$= Q3 \cdot \overline{ID} \cdot G2$

A2U21B output $\overline{Q3} \cdot \overline{ID} \cdot G2$

combined output: $\overline{ID}(Q3 \oplus G2)$
(this is called wired OR)

4-90. In divide mode, all four gates are used to accomplish the inclusion of the input data into the data stream. During the time when no data is present on the ID and $\overline{ID}$ lines, logic 1 on the $\overline{ID}$ line disables A2U21C and A2U22A and the feedback and shift register data is combined as explained in Paragraph 4-89 above. When data is present on the ID and $\overline{ID}$ lines, logic 1 on the ID line disables A2U21A and A2U21B. Now A2U21C and A2U22A are enabled and the data is combined in the same manner except that the shift register data is inverted. This is because it is taken from the reciprocal output of A2U8. The effective output of the shift register is determined by the condition (programmed or not) of the feedback tap. The mathematical expressions are:

A1U21C output: $\overline{Q3} \cdot ID \cdot \overline{G2}$

A2U22A output: $Q3 \cdot ID \cdot G2$

combined output (wired OR) $\overline{ID(Q3 \oplus G2)}$

combined outputs, all four gates: (ORed at the input of A2U29) $ID \oplus Q3 \oplus G2$

4-91. MULTIPLY ENABLE GATE. (Schematic 5.)

4-92. The multiply enable gate, consisting of A1Q12 and A1Q13, is a schmitt trigger whose threshold is determined by voltage divider A1R29/A1R30. The gate provides a bounce-free signal to the multiply gate in multiply mode.

4-93. In NORM or DIVIDE, logic 1 on the $\overline{MULT}$ turns A1Q12 on and A1Q13 turns off holding the MULT line to logic 0.

4-94. In MULTIPLY, logic 0 on the $\overline{MULT}$ line turns A1Q12 off and A1Q13 turns on. The MULT line is now logic 1.

4-95. MULTIPLY GATE. (Schematic 4.)

4-96. The multiply gate, consisting of A2U21B, A2U21C and A2U12C, determines the input function of A2U10. In divide and norm mode, A2U10 is the first cell in the shift register and it's output drives the feedline to the feedback taps. In MULTIPLY, A2U10 serves only to buffer the input data before driving the feedline.

4-97. In norm and divide mode, logic 0 on the MULT line is inverted by A2U12B, disabling A2U12C. Logic 0 on the MULT line enables A2U22B and A2U22C. These gates perform the function performed by the exclusive NOR gates between the shift register cells Q20 through Q3.

4-98. In multiply mode, logic 1 on the MULT line disables A2U22B and A2U22C. Logic 1 on the MULT line is inverted by A2U12B, enabling A2U12C and permitting data on the $\overline{IM}$ line to pass (inverted) to the D input of A2U10.

4-99. The mathematical expressions for the multiply gate are:

A2U22B output: $Q2 \cdot \overline{MULT} \cdot \overline{G1}$

A2U22C output: $\overline{Q2} \cdot \overline{MULT} \cdot G1$

A2U21C output: $MULT \cdot IM$

Combined output:
(wired OR)

$MULT(Q2 + G1) + M \cdot IM + Q1 \cdot Z$

4-100. ZERO DETECTOR. (Schematic 4.)

4-101. The zero detector is used to establish a repeatable trigger point once each cycle of the PR sequence and to prohibit the all zero condition. The trigger pulse is needed to stabilize an oscilloscope display. The all zero condition is self-sustaining and a means is reguired to re-establish normal operation when the condition occurs.

4-102. The outputs of shift register cells Q20 through Q2 are monitored (monitor 1 through monitor 6) at the inputs of OR gate A2U14. When the inputs to the OR gate are all logic 0, it's output is logic 0 and one of two actions occur.

4-103. If the Q output of A2U10 is logic 1, the logic 1 is inverted by the NOR sections of A2U16A and A2U15C is enabled. Logic 1 then appears on the TRIGGER line.

4-104. If the Q output of A2U10 is logic 0, the OR output of A2U16A will be logic 0 and A2U15D will be enabled. A2U15D is wired ORed to the output of the multiply gate and the logic 1 on it's output will be loaded into the input of A2U10 enabling operation of the shift register to resume.

4-105. Mathematically, the functions of the zero detector may be expressed as follows:

$$Q2 + Q3 + Q4 \cdots Q20 = \overline{Z}$$

A2U15C output: $Q1 \cdot Z$

A2U15D output: $\overline{Q1} \cdot Z$

4-106. DATA COMPARATOR. (Schematic 4.)

4-107. The Model 1930A can be used to measure digital errors in an incoming data stream. The multiply circuits are used to synchronize to the incoming sequence and the data comparator is used to detect errors between the incoming data and the self-generated sequence. Because flip-flop A2U10 is used to buffer the incoming data, the synchronized sequence will be delayed by one bit from the incoming sequence. Comparison is made between the incoming sequence (in norm and multiply mode) and the internal sequence advanced one bit. The one bit advance, made to offset the one bit delay previously described, is accomplished by comparing the input to A2U11 with the data signal ($\overline{IM}$) at A2U24B. As long as the incoming sequence is correct, the inputs to A2U24B will be equal and the output of the gate will be logic 1. If an instantaneous error occurs (usually a noise pulse), for the duration of the error, the output of A2U24B will fall to logic 0 and one clock pulse later appears on the ERROR line. The use of A2U23 to buffer the output of A2U24B cleans up the error pulses and delays them one bit in time so that they occur synchronized with the internally generated sequence and one bit delayed from the incoming sequence.

4-108. The output of A2U24A is: Q2 + G2 which corresponds to PRBS advanced one bit in time.

4-109. The output of A2U24B is: IM + Q2 + G2 which corresponds to the instantaneous logic errors between the internally generated sequence and the incoming sequence.

4-110. FEEDLINE.

4-111. The feedline is not fed directly from the output of A2U10. The shift register is located on two PC boards, A2 (Schematic 4) and A3 (Schematic 3). Each board has a separate feedline isolated from the output of A2U10 by emitter followers: A2Q1 and A2Q2 on board A2 and A3Q1 and A3Q2 on board 3.

4-112. OUTPUT GATE. (Schematic 5.)

4-113. In norm and divide mode, PRBS OUTPUT comes from the last shift register cell. In multiply mode, PRBS OUTPUT comes from the data comparator. The switching takes place in the output gate circuitry A1U3A, A1U3B and A1U3C.

4-114. In norm and divide mode, logic 1 on the $\overline{MULT}$ disables A1U3C. Logic 1 on the $\overline{MULT}$ is inverted by A1U3A, enabling A1U3B which passes data on the $\overline{PRBS}$ line to the base of A1Q14.

4-115. In multiply mode, logic 0 on the $\overline{MULT}$ line is inverted by A1U3A, disabling A1U3B. Logic 0 on $\overline{MULT}$ line enables A1U3C, permitting data on the $\overline{ERROR}$ line to pass to the base of A1Q14.

4-116. If the NRZ^1 line is logic 0, the output of A1U21C will be held at logic 0 and the data will pass through A1U3B or A1U3C unchanged; that is, in NRZ format. If the NRZ^1 line is logic 1, the output of A1U21C will be $\overline{CL}$ pulses and the output of A1U3B or A1U3C will be gated clock pulses.

4-117. The mathematical expressions for the gate function is:

$$(MULT \quad PRBS + M \quad ERROR)(CL + NRZ^1)$$

4-118. RZ/NRZ GATE.

4-119. The RZ/NRZ gate consists of A1U2B, A1U2C and A1U2D. The function for NRZ^1 was explained in Paragraph 4-116 above.

4-120. A1U2D performs the same function for error pulses entering the error buffer amplifier that A1U2C performs for PRBS. As wired in the factory, the error output is always RZ because the NRZ^2 line is not connected. If NRZ output from ERROR OUTPUT is desired, connect A5P1-13 to A5P1-14. The RZ/NRZ switch will then control the formatting function for both outputs.

4-121. OUTPUT BUFFER AMPLIFIERS. (Schematic 5.)

4-122. The buffer amplifiers reshape, amplify, and change the levels of the three output signals PRBS, ERROR and TRIGGER. Each circuit consists of two cascaded emitter-coupled amplifiers. The first amplifier is driven single-ended from an ECL gate. The output of the first amplifier drives the input of the second amplifier differentially.

The differential drive cleans common mode noise from the waveform and decreases the rise and fall times. The second amplifier drives a 50-ohm transmission line single-ended to the output connector.

4-123. PRBS BUFFER AMPLIFIER. Consists of A1Q14, A1Q15, A1Q16 and A1Q17. Input is to the base of A1Q14 and output is from the collector of A1Q15.

4-124. ERROR BUFFER AMPLIFIER. A1Q18, A1Q19, A1Q20, A1Q21 and A1Q22. Output is from the collector of A1Q20. A1Q18 and A1Q21 are in parallel and are made to function as an AND gate. Normally, both transistors are saturated so that the voltage at the base of A1Q19 cannot rise unless the current in both A1Q18 and A1Q21 is decreased simultaneously. This happens when an error pulse and a clock pulse are applied simultaneously to their bases, creating a pulse at the output whose width is limited to the width of a clock pulse. If the instrument is modified to permit NRZ error pulse output, then logic 0 will be at the output of A1U2D and the base of A1Q18. This will cut-off A1Q18 and the input will function as if it were not in the circuit.

4-125. TRIGGER BUFFER AMPLIFIER. Consists of A1Q31, A1Q32, A1Q29, A1Q30. Input is to the base of A1Q31 and output is from the collector of A1Q29.

4-126. SYNC INDICATOR. (Schematic 5.)

4-127. When the Model 1930A is synchronized to an external sequence, the errors will drop from 1/2 the clock rate to a much lower value determined by the number of errors (usually noise) in the incoming signal. This drop in error rate is used to indicate synchronization. The threshold of the circuit is an error rate of about 2×10^{-2}.

4-128. When an error occurs, the error pulse will discharge A1C19 through A1R37 and A1Q23. If there are no errors the capacitor will be charged by the base current of A1Q24. When the base of A1Q24 rises to a higher voltage than the base of A1Q25, A1Q24 will turn off and A1Q25 will turn on, and in turn, turn on A1Q26. A1Q26 will drive the sync lamp.

4-129. On the other side of the circuit, A1Q27 will turn off along with A1Q24 and A1Q28. The collector of A1Q28 will rise to +4.1 volts to indicate SYNC to the attached programming unit (if any).

4-130. The sync indication will be ambiguous if the clock rate is less than 100 Hz or if the error rate is much greater than 3×10^{-2}. When the clock is very slow, the sync lamp will turn on during long strings of zeros. If the clock is not present, and the output of the last shift register cell happens to be stopped on zero, the lamp will light. When the error rate is high, the circuit will not indicate sync even though the error free sequences are synchronized.

4-131. PROGRAMMING CIRCUIT. (Schematic 6.)

4-132. Program enable is made by the REGISTER LENGTH switch on the front panel. The programming circuits are located on program board A4. The circuits on A4 also interface between DTL logic levels (+4/0 volts) and MECL logic levels (−0.7/−1.5 volts) and select the proper gates in the front panel PRBS mode.

4-133. When REGISTER LENGTH switch is not in PGM, the PGM enable line is open. This causes A4Q3 and A4Q4 to turn on and A4Q1 and A4Q2 to turn off. With A4Q4 on, −4.6 volt enabling signals are provided through A4CR27, A4CR28 and A4CR29 to the MULTIPLY/NORM/DIVIDE, RZ/NRZ and RESET switches on the front panel.

4-134. Both sides of the resistor network are held at logic 1 (−0.6 volt). The outputs of the resistor networks remain at logic 1 until pulled to logic 0 (−1.5 volts) by a front panel switch.

4-135. SWITCH OPERATION. (Schematic 1.) Operation of the front panel mode switches is as follows:

4-136. When the PRBS/WORD switch is in WORD, logic 0 is sent to the feedback tap whose number is the same as the REGISTER LENGTH switch. For instance, if the REGISTER LENGTH switch is set to 5, logic 0 will be routed (hard wired) to $\overline{K5}$ on board A2. When the switch is in the PRBS position, logic 0 will be sent on the appropriate PRBS line to diode logic on board A4. The diodes will then route logic 0 to the appropriate feedback taps on boards A2 and A3.

4-137. When the MULTIPLY/NORM/DIVIDE switch is in MULTIPLY, logic 0 is sent to the $\overline{\text{MULT}}$ line on board A1. In DIVIDE, logic 0 is sent to the $\overline{\text{DIV}}$ line. In NORM, no signal is sent, therefore logic 1 appears on both the $\overline{\text{MULT}}$ and $\overline{\text{DIV}}$ lines.

4-138. When the RZ/NRZ switch is in RZ, logic 0 is sent on the NRZ^1 line. If the instrument has been modified to permit NRZ error output, logic 0 also appears on the NRZ^2 line.

4-139. To program the instrument, the REGISTER LENGTH switch is switched to PGM putting −5.2 volts on the PGM enable line and turning A4Q1 and A4Q3 on. The top of the resistor network will be +25 volts and the bottom will be −4 volts. If a program input is either open or driven from a high voltage (+4 volts), the DTL inter-

face diodes (A4CR1 - A4CR24) will be reverse biased. The appropriate resistor network output will be logic 1. If the program input is grounded, the loss of current will cause the resistor output to fall to logic 0.

4-140. Since A4Q4 is off, diodes A4CR27, A4CR28 and A4CR29 will be reverse biased and the front panel switches will be ineffective.

4-141. The feedback taps are programmed from the outputs of the resistor network.

4-142. In PRBS mode, the feedback taps are enabled from the outputs of the resistor network in both front panel and programmed operation. $\overline{\text{DIV}}$, $\overline{\text{MULT}}$, NRZ and RESET are enabled from the resistor network only in programmed operation. The outputs from the appropriate resistor networks are routed through A5J4 to the various control lines on boards A1, A2 and A3.

Table 5-1. Recommended Test Equipment

Instrument		Required Characteristics	Required For
Type	Model		
High-frequency and Sampling Oscilloscope	HP 140A Mainframe HP 1402A Vert. Ampl. HP 1401A Vert. Ampl. HP 1421A Time Base HP 1425A Time Base	Real Time: VERT. – 20 MHz Sweep – 1 usec/div Sampling: VERT. – 1 ns risetime Sweep – .1 usec/div	Performance Check and Troubleshooting
Mainframe	HP 1900-series	Power source: ±25 Vdc –10 Vdc	Performance check and Troubleshooting
Clock Generator	HP 1906A Rate Generator	60 MHz Rate Output with external input	Performance check and Troubleshooting
Calibrated oscillator	HP 3200B	1 MHz – 60 MHz 1 volt into 50 ohms	Performance Check
Electronic counter	HP 5345L/M	50 MHz rep rate Time base output	Performance Check
50 ohm load	HP 10100A		Performance Check
Cables, 50 ohm w/BNC connectors	HP 10503A	Non-reactive connectors	Performance Check and Troubleshooting
Tee connectors, 50 ohms	HP 1250-0781	BNC Connection	Performance Check and Troubleshooting
10X Pad	General Radio Type 874	20 dB attenuation	Performance Check
OPTIONAL TEST EQUIPMENT:			
Delay Generator	HP 1910A	Adjustable 25 ns delay	Alternate Performance Check
Pseudo Random Binary Sequence Generator	HP 1930A	Refer to Table 1-1	Alternate Performance Check

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SECTION V

PERFORMANCE CHECK AND ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section contains step-by-step procedures for checking the instrument specifications as given in Table 1-1 of this manual. The performance check procedure gives troubleshooting suggestions in case the instrument fails to meet any specification tested. A table (performance check record) is provided at the end of the performance check for recording the measurements obtained in the first running of the procedure. This record may be used to compare measurements taken at later dates with the original. The procedures for making all internal adjustments are covered in Paragraphs 5-19 through 5-22.

5-3. TEST EQUIPMENT.

5-4. Test equipment recommended for procedures in this section is listed in Table 5-1. Test equipment equivalent to that recommended may be substituted, provided it meets the required characteristics listed in the table. For best results, use recently calibrated test equipment.

5-5. PERFORMANCE CHECK.

5-6. Paragraphs 5-10 through 5-14 describe procedures to determine whether or not the instrument is operating within the specifications of Table 1-1. This check can be used as part of an incoming inspection, as a periodic operational test, or to check calibration after repairs or adjustments have been made. Any one of the following checks can be made separately if desired.

5-7. The first time the performance check is made, enter the results on the Performance Check Record at the end of the procedure. Remove the record from the manual and file it for future reference. Be sure to include the instrument serial number on the record for identification.

5-8. Paragraphs 5-16 through 5-18 contain functional checks whose characteristics are not specified in Table 1-1. Since these characteristics are not specified, stated results are approximate.

5-9. SPECIFICATION CHECKS.

5-10. MAXIMUM CLOCK RATE.

a. Connect equipment as shown in Figure 5-1.

b. Set Model 1930A front-panel controls as follows:

PRBS/WORD . . . . . PRBS
MULTIPLY/NORM/DIVIDE . . . . . NORM
RZ/NRZ . . . . . NRZ
REGISTER LENGTH 3

c. Set output of calibrated oscillator and clock generator to 35 MHz.

d. Set oscilloscope to observe a 2-volt, 7 bit sequence.

e. Observe pattern on oscilloscope. Note relative positions of true bits.

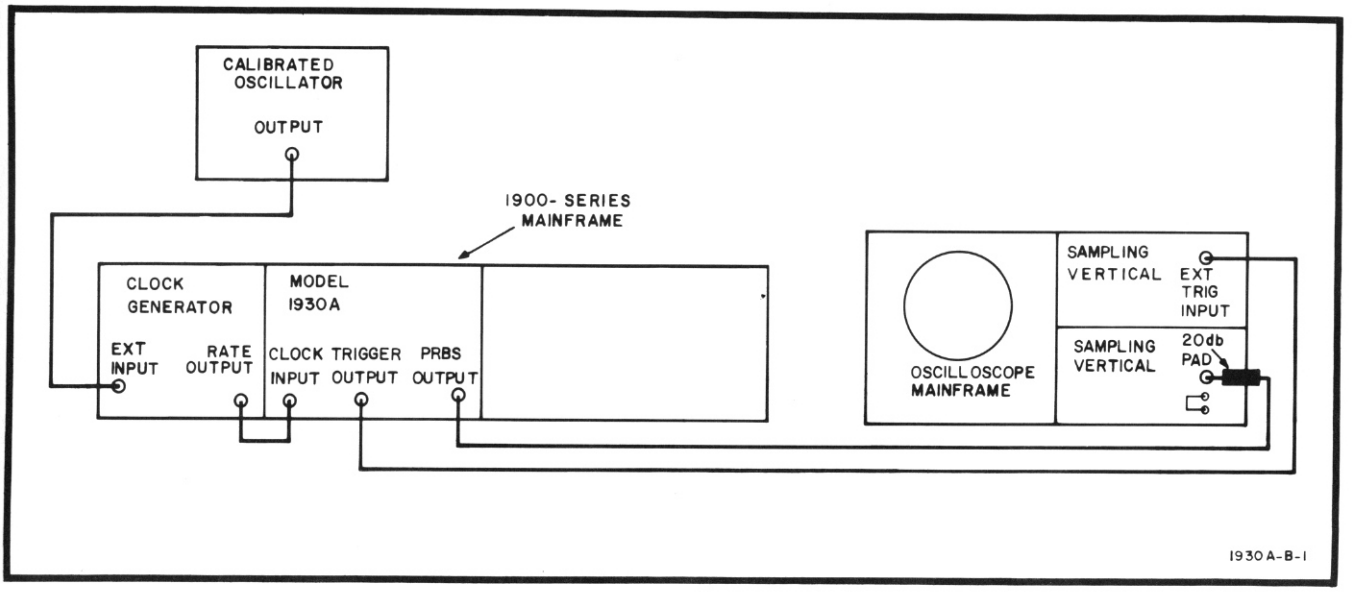


Figure 5-1. Maximum Clock Rate Test, Part I.

f. Slowly increase frequency output of calibrated oscillator/clock generator. Pattern on oscilloscope will compress as frequency is increased but relative positions of bits should be constant.

g. At some frequency, the pattern will abruptly change or cease altogether.

h. Slightly decrease frequency until pattern is restored. This is the maximum repetition rate.

i. Repeat steps c through h for REGISTER LENGTH 5, 7 and 10. Determine maximum repetition rate for each position.

j. Connect equipment as shown in Figure 5-2.

k. Set Model 1930A front-panel controls as in step b except that REGISTER LENGTH switch is set to 11.

l. Set counter for period. Adjust time base for four digits.

m. Set calibrated oscillator/clock generator for 35 MHz output and observe reading.

n. Increase frequency of calibrated oscillator and observe period decrease as frequency is increased.

o. At some frequency, the period will suddenly change or stop altogether.

p. Slightly reduce clock frequency until stable reading is restored. This is maximum clock repetition rate.

q. Repeat steps m through p in all REGISTER LENGTH positions, 13 through 20. Determine maximum repetition rate in each position.

r. Maximum repetition rate in all REGISTER LENGTH positions, 3 through 20, shall be greater than 40 MHz.

s. If specification listed in step r is not met, perform adjustment described in Paragraph 5-23.

5-11. MAXIMUM CLOCK RATE (Alternate Method).

a. Connect equipment as shown in Figure 5-3.

b. Set Model 1930A (under test) front-panel controls as follows:

PRBS/WORD	PRBS
MULTIPLY/NORM DIVIDE	NORM
RZ/NRZ	NRZ
REGISTER LENGTH	3

c. Set Model 1930A (test unit) front-panel controls as follows:

PRBS/WORD	PRBS
MULTIPLY/NORM/DIVIDE	MULTIPLY
RZ/NRZ	NRZ
REGISTER LENGTH	3

d. Set delay generator for 25 ns delay.

e. Set calibrated oscillator/clock generator to 35 MHz.

f. Observe SYNC lamp. It should be lit.

g. Increase clock frequency until SYNC lamp goes out.

h. Try to cause SYNC lamp to re-lite by slightly varying delay from delay generator.

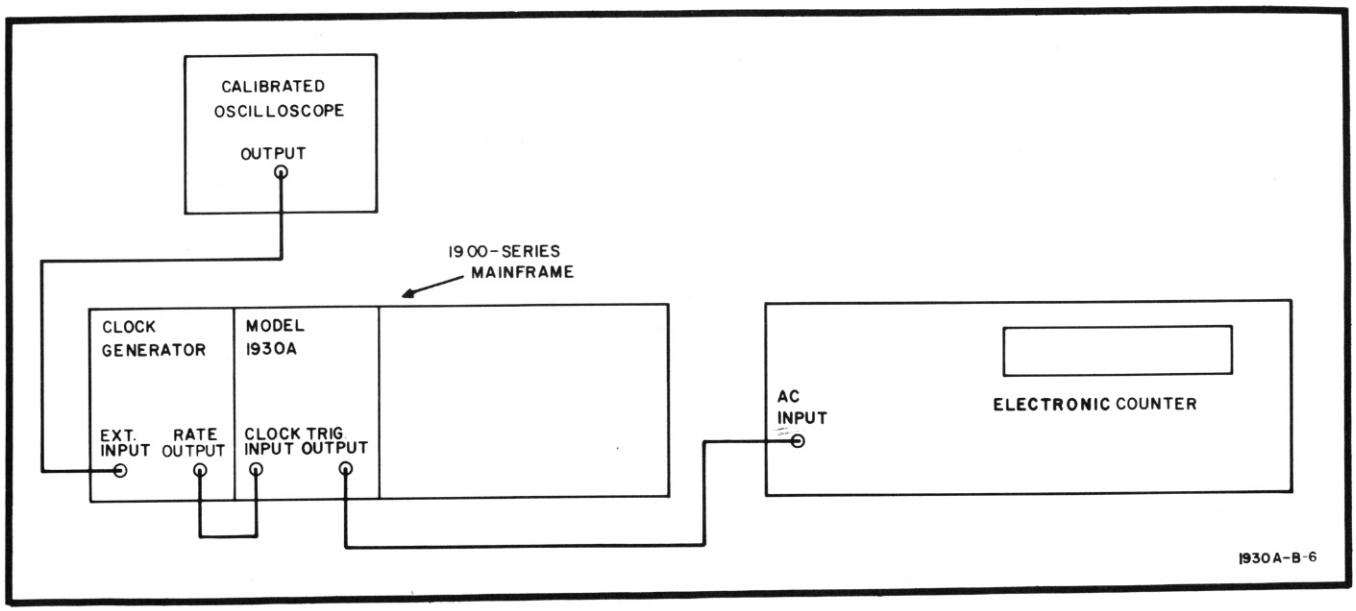


Figure 5-2. Maximum Clock Rate Test, Part II.

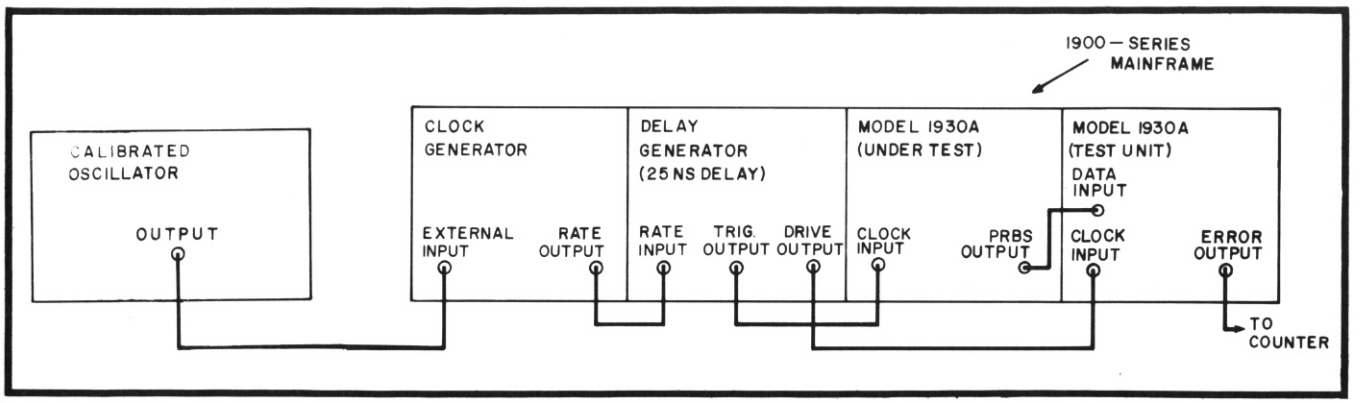


Figure 5-3. Maximum Clock Rate Test, Alternate Method.

i. When the clock frequency has been increased to the point where further adjustments of delay will not cause SYNC lamp to re-light, slightly reduce clock frequency until SYNC lamp lights. This is the maximum clock repetition rate.

j. Switch REGISTER LENGTH on both Model 1930A's to positions 5 through 20. Determine the maximum repetition rate for each position.

k. Maximum clock repetition rate for each REGISTER LENGTH position shall be greater than 40 MHz.

5-12. PRBS OUTPUT.

a. Connect equipment as shown in Figure 5-4.

b. Set Model 1930A front-panel controls as follows:

PRBS/WORD ..... PRBS
MULTIPLY/NORM/DIVIDE ..... NORM
RZ/NRZ ..... NRZ
REGISTER LENGTH 3

c. Adjust oscilloscope to observe single PRBS pulse.

d. Amplitude of pulse shall be > 2V. Rise and fall times shall be less than 4 ns. Width shall be approximately 1 clock period (time between two adjacent clock pulses).

e. Switch RZ/NRZ to RZ. Pulse width shall be > 9 ns, < 50% of period.

5-13. TRIGGER OUTPUT.

a. Repeat Paragraphs 5-12a and 5-12b while observing pulse at TRIGGER OUTPUT.

b. Amplitude of pulse shall be greater than 0.5V. Width shall be approximately 1 clock period.

5-14. ERROR OUTPUT.

a. Repeat paragraphs 5-12a and 5-12b while observing pulse at ERROR OUTPUT.

b. Amplitude shall be > 2V. Width shall be > 10 ns, < 50% of period.

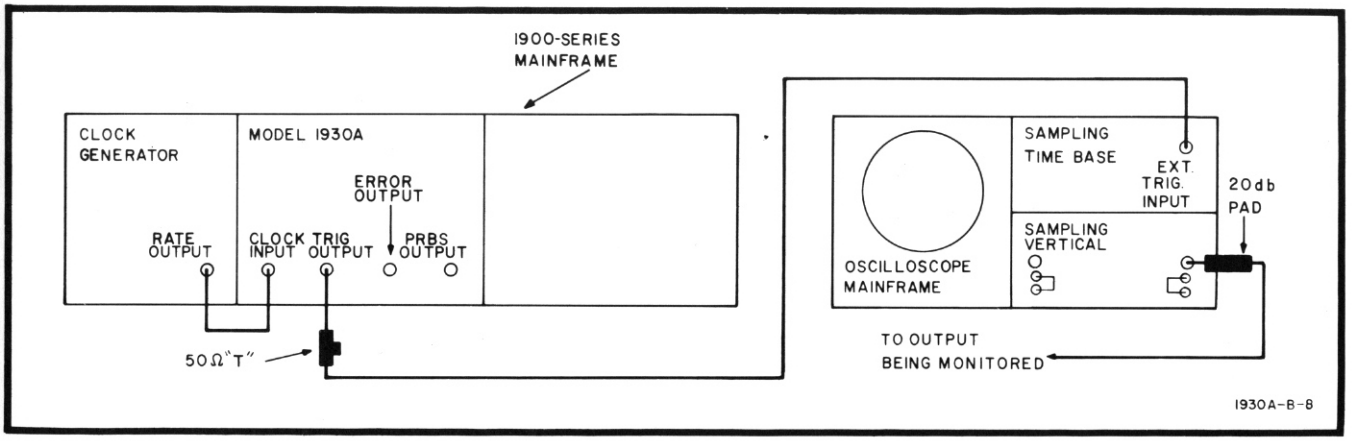


Figure 5-4. Pulse Checks

5-15. FUNCTIONAL CHECKS.

5-16. MULTIPLY/NORM/DIVIDE.

a. Connect equipment as shown in Figure 5-5.

b. Set Model 1930A front-panel controls as follows:

PRBS/WORD . . . . . Figure 5-6
MULTIPLY/NORM/DIVIDE . . . . . Figure 5-6
RZ/NRZ . . . . . NRZ
REGISTER LENGTH 3

c. Set clock generator to 1 MHz.

d. Set PRBS/WORD and MULTIPLY/NORM/DIVIDE as shown in Figure 5-6 and observe indicated pattern on oscilloscope.

NOTE

While monitoring Model 1930A PRBS OUTPUT with channel B of the oscilloscope, the length of the work or PRBS can be determined by monitoring Model 1930A TRIGGER OUTPUT on channel A and comparing the two displays. Word or PRBS length is the time between two adjacent trigger pulses. To determine the number of bits (period) in the word or PRBS, monitor the output of the clock generator with channel A. The time between two adjacent clock pulses is one period.

5-17. WORD AND SEQUENCE LENGTH.

a. Connect equipment as shown in Figure 5-7.

b. Set time base of counter to 0.1 us and function for a period average of 1.

c. Set Model 1930A front-panel controls as follows:

PRBS/WORD . . . . . WORD
MULTIPLY/NORM/DIVIDE . . . . . NORM
RZ/NRZ . . . . . NRZ

d. Observe counter reading at each position of REGISTER LENGTH switch. Press RESET switch before each reading. Counter should read same as REGISTER LENGTH switch.

e. Switch PRBS/WORD to PRBS.

f. Observe reading for each position of REGISTER LENGTH switch. Readings should be as shown for starred values in Table 3-3.

5-18. PROGRAMMED OPERATION.

a. Connect equipment as shown in Figure 5-8.

b. Set REGISTER LENGTH switch to PGM.

c. Program MULTIPLY $\overline{K1}$ and RESET. (See Figure 3-5 and Paragraph 3-70).

d. Monitor PRBS OUTPUT. Output should be pulse train of period 2. Amplitude of pulses should be about 2 volts peak-to-peak.

e. Open $\overline{K1}$ and program $\overline{K2}$. Output should be pulse train of period 3.

f. Continue programming individual feedback taps. Word length should continue stretching until at $\overline{K20}$ it will be 21 bits (period 21) long.

g. Leaving $\overline{K20}$ programmed, also program $\overline{K1}$. First bit in serial word should be true.

h. Leaving $\overline{K1}$ and $\overline{K20}$ programmed, also program $\overline{K2}$. Second bit in word should be true.

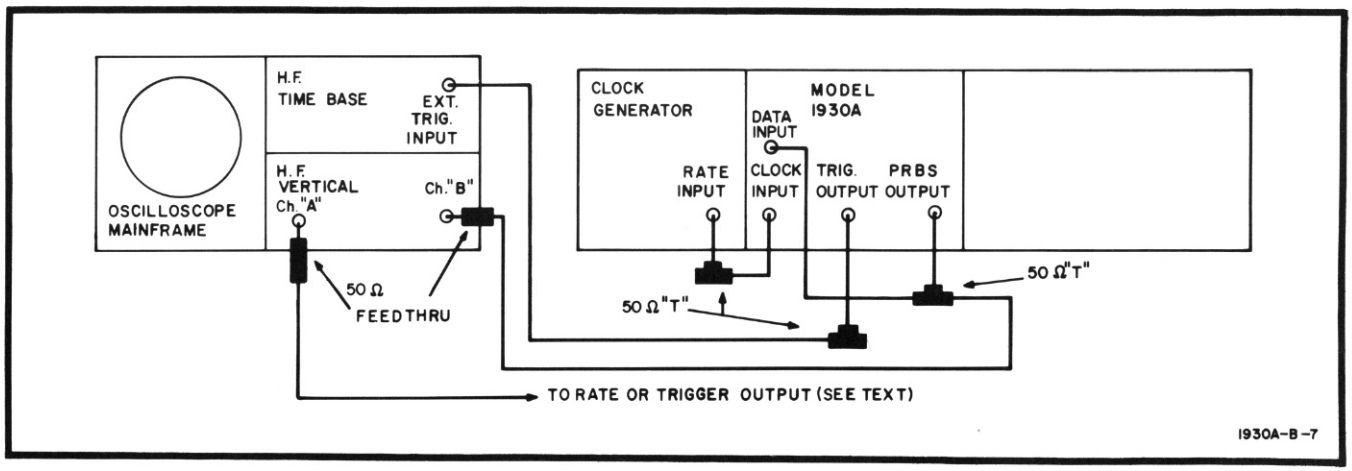


Figure 5-5. Multiply/norm/divide Test.

PRBS/WORD	MULTIPLY/NORM/DIVIDE	PATTERN	WAVEFORM
WORD	MULTIPLY	111101011001000	A
PRBS	NORM	1110010	B
WORD	DIVIDE	1110010	C

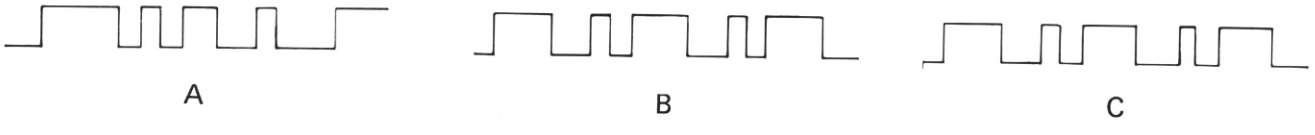


Figure 5-6. Function Patterns.

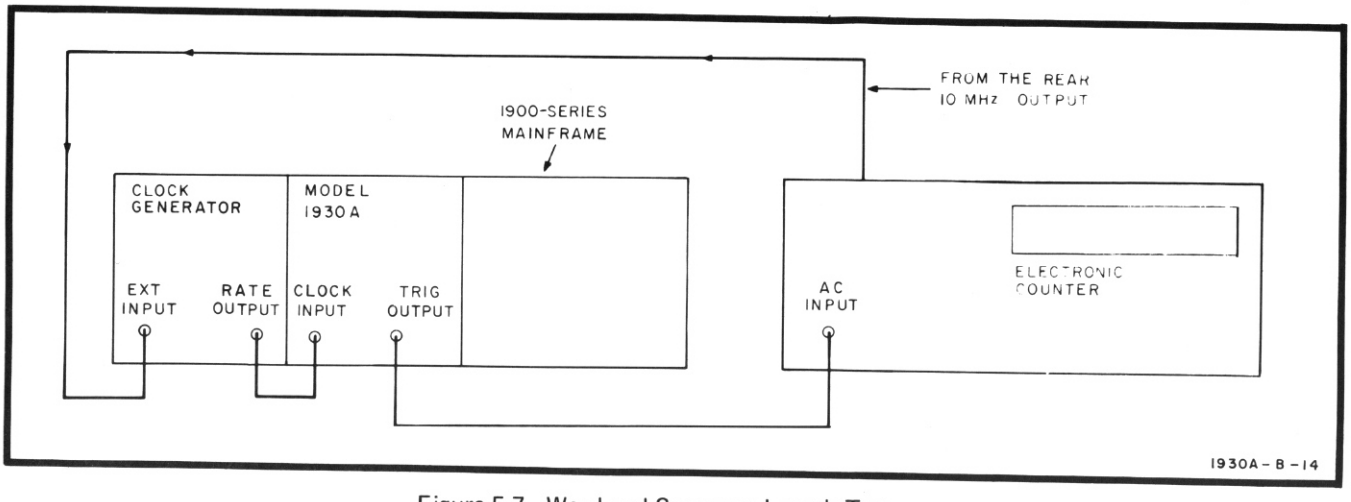


Figure 5-7. Word and Sequence Length Test.

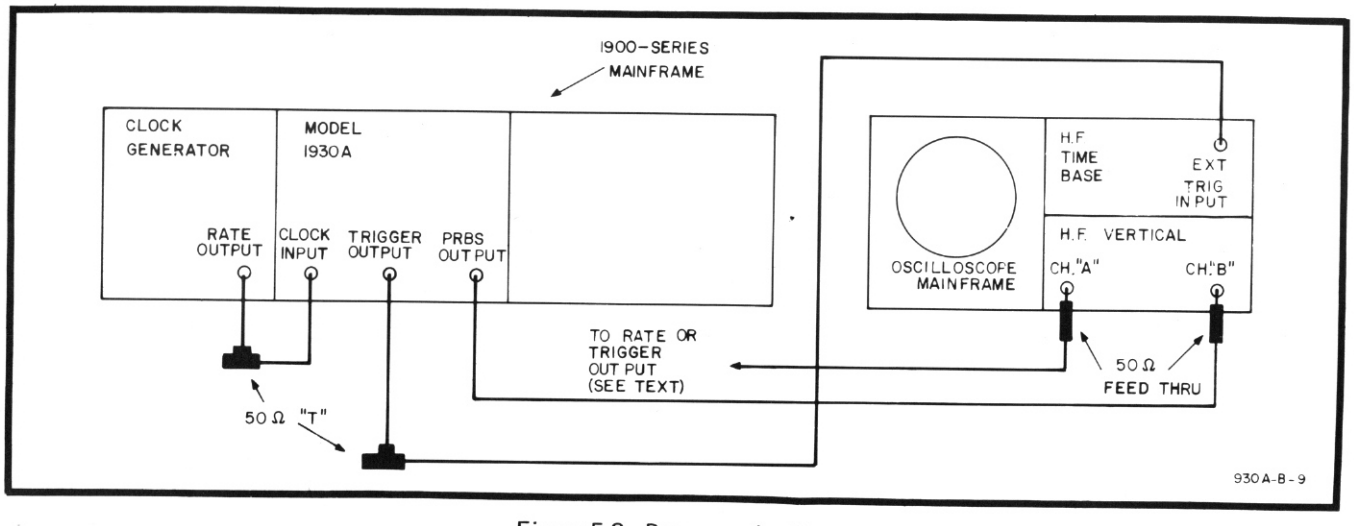


Figure 5-8. Programming Tests.

i. Continue in this fashion until all feedback taps are programmed on. Ensure that true bits in word follow feedback taps as they are programmed.

j. Open all feedback taps and $\overline{\text{MULT}}$.

k. Program $\overline{\text{K3}}$ and $\overline{\text{K5}}$. Observe randon looking sequence of period 31.

l. Open RESET. All true bits should go to 0.

m. Leaving $\overline{\text{K3}}$ and $\overline{\text{K5}}$ programmed, program RZ and MULTIPLY. Ensure that output is series of spikes within the envelope of previous NRZ pulse train.

n. If trouble is encountered in above procedure, see steps 9 through 13 in Figure 8-1.

5-19 SELF GENERATED ERROR RATE.

5-20 The self generated error rate of the 1930A may be checked by using two 1930A PRPS generators which are set to the same sequence e. g. $2^{20} - 1$ (Figure 5-3). Connect the Output of the first generator to the Data Input of the second generator. Drive the first generator with the trigger output of a 1910A delay generator which has been set for a delay of 25 ns. Drive the second generator with the delay output of the delay generator. Set the clock frequency to 40 MHz. Count the error output pulses of the second generator with an events counter. Make sure there are no power line drop outs during this test. The self generated error rate will then be:

$$\text{Error Rate} = \frac{(\text{number of errors}) \times 6.94 \times 10^{-12}}{(\text{hours tested})}$$

$$\text{Error Rate} = \frac{(\text{number of errors}) \times 2.89 \times 10^{-13}}{(\text{days tested})}$$

5-21 ADJUSTMENTS.

5-22 The Model 1930A has only one adjustment. BIAS ADJ A1R9, used to obtain maximum repetition rate, is located beneath a screwdriver access hole near the left front corner of the top cover.

5-23 Use recently calibrated test equipment with characteristics as specified in Table 5-1. After the adjustment is completed, check instrument performance by doing the performance check at the beginning of this section.

5-24. ADJUSTMENT

a. Connect equipment as shown in Figure 5-1. For the clock source, use the most narrow pulse width generator available.

b. Set Model 1930A front-panel controls as follows:

PRBS/WORD	PRBS
MULTIPLY/NORM/DIVIDE	NORM
RZ/NRZ	NRZ
REGISTER LENGTH	5

c. Stabilize pattern on oscilloscope and note bit distribution of pattern.

d. Slowly increase frequency of calibrated oscillator until the pattern changes.

e. Engage A1R9 with thin insulated screwdriver and adjust until original pattern is restored.

f. Repeat d and e above until further tuning of A1R9 will not restore original pattern or sequence stops.

g. Slightly decrease frequency until original pattern can be restored. This frequency is the maximum repetition rate for the instrument. It shall be greater than 40 MHz.

PERFORMANCE CHECK RECORD

1930A

Instrument Serial Number _____ **Date** _____

Check		Specification	Measured
Maximum Clock Rate:	3	40 MHz	
	5	40 MHz	
	7	40 MHz	
	10	40 MHz	
	11	40 MHz	
	13	40 MHz	
	15	40 MHz	
	16	40 MHz	
	17	40 MHz	
	19	40 MHz	
	20	40 MHz	
PRBS Pulse	Amplitude	> 2V	
	Risetime	<4 ns	
	Falltime	<4 ns	
	Width RZ	> 9 ns, < 50% of period	
Trigger Pulse:	Amplitude	>1V	
	Width	1 clock period	
Error Pulse:	Amplitude	>2V	
	Width	>10 ns, <50% of period	
Multiply/Norm/Divide		OK	
Word and Sequence Length		OK	
Programmed Operation		OK	

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. The abbreviations used in the parts list are described in Table 6-1. Table 6-2 lists the parts in alphanumeric order by reference designator and includes the manufacturer and manufacturer's part number. Table 6-3 contains the list of manufacturer's codes.

6-3. ORDERING INFORMATION.

6-4. To obtain replacement parts from Hewlett-Packard, address order or inquiry to the nearest Hewlett-Packard Sales/Service Office and supply the following information:

a. Instrument model and serial number.

b. HP Part Number of item(s).

c. Quantity of part(s) desired.

d. Reference designator of part(s).

6-5. To order a part not listed in the table, provide the following information:

a. Instrument model and serial number.

b. Description of the part, including function and location in the instrument.

c. Quantity desired.

Table 6-1. Abbreviations for Replaceable Parts List

A	= ampere(s)
ASSY	= assembly
BD	= board(s)
BH	= binder head
BP	= bandpass
C	= centi (10^{-2})
CAR	= carbon
CCW	= counterclockwise
CER	= ceramic
CMO	= cabinet mount only
COAX	= coaxial
COEF	= coefficient
COMP	= composition
CONN	= connector(s)
CRT	= cathode-ray tube
CW	= clockwise
D	= deci (10^{-1})
DEPC	= deposited carbon
DP	= double pole
DT	= double throw
ELECT	= electrolytic
ENCAP	= encapsulated
EXT	= external
F	= farad(s)
FET	= field-effect transistor(s)
FH	= flat head
FIL H	= fillister head
FXD	= fixed
G	= giga (10^{9})
GE	= germanium
GL	= glass
GRD	= ground(ed)
H	= henry(ies)
HG	= mercury
HP	= Hewlett-Packard
HZ	= hertz
IF	= intermediate freq.
IMPG	= impregnated
INCD	= incandescent
INCL	= include(s)
INS	= insulation(ed)
INT	= internal
K	= kilo (10^{3})
KG	= kilogram
LB	= pound(s)
LH	= left hand
LIN	= linear taper
LOG	= logarithmic taper
LPF	= low-pass filter(s)
LVR	= lever
M	= milli (10^{-3})
MEG	= mega (10^{6})
MET FILM	= metal film
MET OX	= metal oxide
MFR	= manufacturer
MINAT	= miniature
MOM	= momentary
MTG	= mounting
MY	= mylar
N	= nano (10^{-9})
N/C	= normally closed
NE	= neon
N/O	= normally open
NPO	= negative positive zero (zero temperature coefficient)
NPN	= negative-positive-negative
NSR	= not separately replaceable
OBD	= order by description
OH	= oval head
OX	= oxide
P	= peak
PC	= printed (etched) circuit(s)
PF	= picofarads
PHL	= Phillips
PIV	= peak inverse voltage(s)
PNP	= positive-negative-positive
P/O	= part of
PORC	= porcelain
POS	= position(s)
POT	= potentiometer(s)
P-P	= peak-to-peak
PRGM	= program
PS	= polystyrene
PWV	= peak working voltage
RECT	= rectifier(s)
RF	= radio frequency
RFI	= radio frequency interference
RH	= round head or right hand
RMO	= rack mount only
RMS	= root mean square
RWV	= reverse working voltage
S-B	= slow-blow
SCR	= silicon controlled rectifier
SE	= selenium
SEC	= second(s)
SECT	= section(s)
SI	= silicon
SIL	= silver
SL	= slide
SP	= single pole
SPL	= special
ST	= single throw
STD	= standard
TA	= tantalum
TD	= time delay
TFL	= teflon
TGL	= toggle
THYR	= thyristor
TI	= titanium
TNLDIO	= tunnel diode(s)
TOL	= tolerance
TRIM	= trimmer
U	= micro (10^{-6})
V	= volts
VAR	= variable
VDCW	= dc working volt(s)
W	= watt(s)
W/	= with
WIV	= working inverse voltage
W/O	= without
WW	= wirewound

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	01930-66501	1	BOARD ASSY:IO BUFFER	28480	01930-66501
A1C1	0150-0093	17	C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C2	0180-2203	10	C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A1C3	0180-2204	5	C:FXD ELECT 10 UF 20% 10VDCW	37942	TIM106M010POW
A1C4	0180-2204		C:FXD ELECT 10 UF 20% 10VDCW	37942	TIM106M010POW
A1C5	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C6	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C7	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A1C8	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C9	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A1C10	0180-2204		C:FXD ELECT 10 UF 20% 10VDCW	37942	TIM106M010POW
A1C11	0160-3443	1	C:FXD CER 0.1 UF +80-20% 50VDCW	72982	8131-050-651-104Z
A1C12	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C13	0180-2204		C:FXD ELECT 10 UF 20% 10VDCW	37942	TIM106M010POW
A1C14	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A1C15	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C16	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C17	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C18	0180-2204		C:FXD ELECT 10 UF 20% 10VDCW	37942	TIM106M010POW
A1C19	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A1C20	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C21	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C22	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1C23	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A1CR1	1901-0040	73	DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR2	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR3	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR4	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR5	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR6	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1L1	01925-82701	3	FILTER	28480	01925-82701
A1L2	9100-2259	2	COIL/CHOKE 1.50 UH 10%	99800	1025-24
A1L3	9100-2259		COIL/CHOKE 1.50 UH 10%	99800	1025-24
A1Q1	1853-0006	1	TSTR:SI PNP	80131	2N3134
A1Q2	1854-0205	1	TSTR:SI NPN	80131	2N3904
A1Q3	1853-0084	1	TSTR:SI PNP	80131	2N4918
A1Q4	1853-0015	5	TSTR:SI PNP	80131	2N3640
A1Q5	1853-0036	4	TSTR:SI PNP	80131	2N3906
A1Q6	1853-0015		TSTR:SI PNP	80131	2N3640
A1Q7	1854-0019	1	TSTR:SI NPN	28480	1854-0019
A1Q8	1853-0203	9	TSTR:SI PNP	28480	1853-0203
A1Q9	1853-0015		TSTR:SI PNP	80131	2N3640
A1Q10	1853-0015		TSTR:SI PNP	80131	2N3640
A1Q11	1854-0092	10	TSTR:SI NPN	80131	2N3563
A1Q12	1854-0215	3	TSTR:SI NPN	80131	2N3904
A1Q13	1854-0215		TSTR:SI NPN	80131	2N3904
A1Q14	1854-0092		TSTR:SI NPN	80131	2N3563
A1Q15	1853-0203		TSTR:SI PNP	28480	1853-0203
A1Q16	1853-0203		TSTR:SI PNP	28480	1853-0203
A1Q17	1854-0092		TSTR:SI NPN	80131	2N3563
A1Q18	1854-0092		TSTR:SI NPN	80131	2N3563
A1Q19	1853-0203		TSTR:SI PNP	28480	1853-0203
A1Q20	1853-0203		TSTR:SI PNP	28480	1853-0203
A1Q21	1854-0092		TSTR:SI NPN	80131	2N3563
A1Q22	1854-0092		TSTR:SI NPN	80131	2N3563
A1Q23	1853-0015		TSTR:SI PNP	80131	2N3640
A1Q24	1853-0586	1	TSTR:SI PNP	28480	1853-0586
A1Q25	1853-0086	1	TSTR:SI PNP	80131	2N5087
A1Q26	1854-0071	3	TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q27	1854-0071		TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q28	1854-0071		TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q29	1853-0203		TSTR:SI PNP	28480	1853-0203
A1Q30	1853-0203		TSTR:SI PNP	28480	1853-0203
A1Q31	1854-0092		TSTR:SI NPN	80131	2N3563
A1Q32	1854-0092		TSTR:SI NPN	80131	2N3563
A1R1	0812-0066	1	R:FXD WW 0.33 OHM 5% 2W	28480	0812-0066
A1R2	0684-1211	1	R:FXD COMP 120 OHM 10% 1/4W	01121	CB 1211
A1R3	0684-5621	6	R:FXD COMP 5.6K OHM 10% 1/4W	01121	CB 5621
A1R4	0683-3615	1	R:FXD COMP 360 OHM 5% 1/4W	01121	CB 3615
A1R5	0683-6215	1	R:FXD COMP 620 OHM 5% 1/4W	01121	CB 6215
A1R6	0687-8211	1	R:FXD COMP 820 OHM 10% 1/2W	01121	EB 8211
A1R7	0698-5068	2	R:FXD MET FLM 50 OHM 1% 1/8W	28480	0698-5068
A1R8	0684-1021	2	R:FXD COMP 1000 OHM 10% 1/4W	01121	CB 1021
A1R9	2100-2574	1	R:VAR CERMET 500 OHM 10% LIN 1/2W	28480	2100-2574
A1R10	0684-2221	2	R:FXD COMP 2200 OHM 10% 1/4W	01121	CB 2221

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R11	0757-0898	1	R:FXD FLM 82 OHM 2% 1/8W	28480	0757-0898
A1R12	0690-4711	4	R:FXD COMP 470 OHM 10% 1W	01121	GB 4711
A1R13	0690-4711		R:FXD COMP 470 OHM 10% 1W	01121	GB 4711
A1R14	0684-2221		R:FXD COMP 2200 OHM 10% 1/4W	01121	CB 2221
A1R15	0684-4721	24	R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A1R16	0684-5601	1	R:FXD COMP 56 OHM 10% 1/4W	01121	CB 5601
A1R17	0683-2025	6	R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R18	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R19	0684-2721	2	R:FXD COMP 2700 OHM 10% 1/4W	01121	CB 2721
A1R20	0757-0901	1	R:FXD FLM 110 OHM 2% 1/8W	28480	0757-0901
A1R21	0698-5068		R:FXD MET FLM 50 OHM 1% 1/8W	28480	0698-5068
A1R22	0684-3901	3	R:FXD COMP 39 OHM 10% 1/4W	01121	CB 3901
A1R23	0684-3901		R:FXD COMP 39 OHM 10% 1/4W	01121	CB 3901
A1R24	0684-3901		R:FXD COMP 39 OHM 10% 1/4W	01121	CB 3901
A1R25	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R26	0684-1031	2	R:FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A1R27	0684-1811	2	R:FXD COMP 180 OHM 10% 1/4W	01121	CB 1811
A1R28	0683-7515	1	R:FXD COMP 750 OHM 5% 1/4W	01121	CB 7515
A1R29	0684-1811		R:FXD COMP 180 OHM 10% 1/4W	01121	CB 1811
A1R30	0684-1221	1	R:FXD COMP 1.2K OHM 10% 1/4W	01121	CB 1221
A1R31	0684-1011	10	R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R32	0690-4711		R:FXD COMP 470 OHM 10% 1W	01121	GB 4711
A1R33	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R34	0683-2025		R: FXD COMP 2000 OHM 5% 1/4W	01121	CB-2025
A1R35	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R36	0690-4711		R:FXD COMP 470 OHM 10% 1W	01121	GB 4711
A1R37	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R38	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R39	0684-5611	1	R: FXD COMP 560 OHM 10% 1/4W	01121	CB-5611
A1R40	0684-2231	2	R:FXD COMP 22K OHM 10% 1/4W	01121	CB 2231
A1R41	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R42	0684-5621		R:FXD COMP 5.6K OHM 10% 1/4W	01121	CB 5621
A1R43	0684-2721		R:FXD COMP 2700 OHM 10% 1/4W	01121	CB 2721
A1R44	0683-1315	1	R:FXD COMP 130 OHM 5% 1/4W	01121	CB 1315
A1R45	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R46	0684-5621		R:FXD COMP 5.6K OHM 10% 1/4W	01121	CB 5621
A1R47	0684-5621		R:FXD COMP 5.6K OHM 10% 1/4W	01121	CB 5621
A1R48	0684-4711	1	R:FXD COMP 470 OHM 10% 1/4W	01121	CB 4711
A1R49	0683-1625	1	R:FXD COMP 1600 OHM 5% 1/4W	01121	CB 1625
A1R50	0684-1031		R:FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A1R51	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R52	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R53	0687-1021	1	R:FXD COMP 1000 OHM 10% 1/2W	01121	EB 1021
A1R54	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1R55	0683-5605	1	R:FXD COMP 56 OHM 5% 1/4W	01121	CB 5605
A1R56	0683-2025		R:FXD COMP 2000 OHM 5% 1/4W	01121	CB 2025
A1R57	0684-1011		R:FXD COMP 100 OHM 10% 1/4W	01121	CB 1011
A1S1	3101-1534	1	SWITCH:SL SPST	28480	3101-1534
A1U1	1820-0142	3	INTEGRATED CIRCUIT:4INPUT,2-ORANOR	04713	MC1004P
A1U2	1820-0145	10	INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A1U3	1820-0147	3	INTEGRATED CIRCUIT:ECL 3-INPUT NOR GATE	04713	SC 7011PK
A1VR1	1902-3070	1	DIODE:BREAKDOWN 4.22V 5%	04713	SZ10939-74
A1VR2	1902-3096	1	DIODE BREAKDOWN:5.23V 5% 400 MW	28480	1902-3096
A2	01930-66502	1	BOARD ASSY:CONTROL	28480	01930-66502
A2C1	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A2C2	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M0 5POW
A2C3	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M0 5POW
A2L1	01925-82701		FILTER	28480	01925-82701
A2L2	9140-0158	1	COIL:FXD RF 1 UH 10%	99800	1025-20
A2L3	9100-0368	6	COIL:FXD 0.33 UH 10%	36196	1A-3303M
A2L4	9100-0368		COIL:FXD 0.33 UH 10%	36196	1A-3303M
A2L5	9100-0368		COIL:FXD 0.33 UH 10%	36196	1A-3303M
A2Q1	1853-0203		TSTR:SI PNP	28480	1853-0203
A2Q2	1854-0092		TSTR:SI NPN	80131	2N3563
A2R1	0698-5422	2	R:FXD COMP 5600 OHM 10% 1/8W	01121	BB 5621
A2R2	0698-7482	8	R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-7482
A2R3	0698-9992	7	R:FXD FLM 270 OHM 1/8W	28480	0698-9992
A2R4	0698-9991	8	R:FXD FLM 160 OHM 1/8W	28480	0698-9991
A2R5	0698-7923	2	R: FXD COMP 180 OHM 10% 1/8W	28480	0698-7923
A2R6	0698-7482		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-7482
A2R7	0698-7482		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-7482
A2R8	0698-9992		R:FXD FLM 270 OHM 1/8W	28480	0698-9992
A2R9	0698-7482		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-7482
A2R10	0698-9992		R:FXD FLM 270 OHM 1/8W	28480	0698-9992
A2R11	0698-9991		R:FXD FLM 160 OHM 1/8W	28480	0698-9991

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2R12	0698-7924	5	R: FXD COMP 56 OHM 10% 1/8W	28480	0698-7924
A2R13	0698-7926	3	R: FXD COMP 470 OHM 10% 1/8W	28480	0698-7926
A2R14	0698-5992		R:FXD FLM 270 OHM 1/8W	28480	0698-5992
A2R15	0698-5991		R:FXD FLM 160 OHM 1/8W	28480	0698-5991
A2R16	0698-7482		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-7482
A2R17	0698-7924		R: FXD COMP 56 OHM 10% 1/8W		
A2R18	0698-7924		R: FXD COMP 56 OHM 10% 1/8W	28480	0698-7924
A2R19	0698-7482		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-7924
A2R20	0698-7724		R: FXD COMP 56 OHM 10% 1/8W	28480	0698-7482
A2R21	0698-7923	1	R: FXD COMP 18 OHM 10% 1/8W	28480	0698-7924
A2R22	0698-7926	1	R: FXD COMP 470 OHM 10% 1/8W	28480	0698-7923
A2R23	0698-7924		R: FXD COMP 56 OHM 10% 1/8W	28480	0698-7926
A2R24	0698-7924		R: FXD COMP 56 OHM 10% 1/8W	28480	0698-7924
A2TB1	01930-26502	1	BOARD:BLANK PC	28480	0698-9924
A2U1	1820-0272	21	INTEGRATED CIRCUIT:DIGITAL	28480	01930-26502
A2U2	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U3	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U4	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U5	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U6	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U7	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U8	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U9	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U10	1820-0101		INTEGRATED CIRCUIT: DIGITAL	04713	MC-1034P
A2U11	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U12	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A2U13	1820-0235	6	IC:ECL QUAD EXCLUSIVE NOR GATE	28480	1820-0235
A2U14	1820-0999	1	IC:ECL QUAD-NOR	28480	1820-0999
A2U15	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A2U16	1820-0142		INTEGRATED CIRCUIT:4INPUT,2-OR/NOR	04713	MC1004P
A2U17	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A2U18	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A2U19	1820-0142		INTEGRATED CIRCUIT:4INPUT,2-OR/NOR	04713	MC1004P
A2U20	1820-0235		IC:ECL QUAD EXCLUSIVE NOR GATE	28480	1820-0235
A2U21	1820-0147		INTEGRATED CIRCUIT:ECL 3-INPUT NOR GATE	04713	SC 7011PK
A2U22	1820-0147		INTEGRATED CIRCUIT:ECL 3-INPUT NOR GATE	04713	SC 7011PK
A2U23	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A2U24	1820-0235		IC:ECL QUAD EXCLUSIVE NOR GATE	28480	1820-0235
A3	01930-66503	1	BOARD ASSY:SHIFT REGISTER	28480	01930-66503
A3C1	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A3C2	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035P0W
A3L1	01925-82701		FILTER	28480	01925-82701
A3L2	9100-0368		COIL:FXD 0.33 UH 10%	36196	1A-3303M
A3L3	9100-0368		COIL:FXD 0.33 UH 10%	36196	1A-3303M
A3L4	9100-0368		COIL:FXD 0.33 UH 10%	36196	1A-3303M
A3Q1	1854-0092		TSTR:SI NPN	80131	2N3563
A3Q2	1853-0203		TSTR:SI PNP	28480	1853-0203
A3R1	0698-7926		R: FXD COMP 470 OHM 10% 1/8W	28480	0698-7926
A3R2	0698-7923	1	R: FXD COMP 18 OHM 10% 1/8W	28480	0698-7923
A3R3	0698-7924		R: FXD COMP 56 OHM 10% 1/8W	28480	0698-7924
A3R4	0698-7924		R: FXD COMP 56 OHM 10% 1/8W		
A3R5			R:FXD COMP 5600 OHM 10% 1/8W	28480	0698-7924
A3R6	0698-5422		R:FXD FLM 270 OHM 1/8W	01121	BB 5621
A3R7			R:FXD FLM 160 OHM 1/8W	28480	0698-5992
A3R8	0698-5692		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-9991
A3R9	0698-5991		R:FXD FLM 160 OHM 1/8W	28480	0698-7482
A3R10	0698-7482		R:FXD FLM 270 OHM 1/8W	28480	0698-5991
A3R11	0698-5991		R:FXD FLM 160 OHM 1/8W	28480	0698-5992
A3R12	0698-5992		R:FXD COMP 1.2K OHM 10% 1/8W	28480	0698-5991
A3R13	0698-5991		R:FXD FLM 160 OHM 1/8W	28480	0698-7482
A3R14	0698-7482		R:FXD FLM 270 OHM 1/8W	28480	0698-5991
A3R15	0698-5991		R:FXD FLM 160 OHM 1/8W	28480	0698-5992
A3U1	0698-5992		NOT ASSIGNED	28480	0698-5991
A3U2	0698-5991		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A3U3			INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U4	1820-0145		IC:ECL QUAD EXCLUSIVE NOR GATE	28480	1820-0235
A3U5	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U6	1820-0235		NOT ASSIGNED		
A3U7	1820-0272		NOT ASSIGNED		
A3U8			INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U9			IC:ECL QUAD EXCLUSIVE NOR GATE	28480	1820-0235
A3U10	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
	1820-0235				
	1820-0272				

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A3U11	1820-0272		INTEGRATED CIRCUIT:DIGITAL	C4713	SC 7022PK
A3U12	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A3U13			NOT ASSIGNED		
A3U14			NOT ASSIGNED		
A3U15	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U16	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U17	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A3U18	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A3U19	1820-0145		INTEGRATED CIRCUIT:DIGITAL QUAD	04713	SC7010PK
A3U20	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U21	1820-0235		IC:ECL QUAD EXCLUSIVE NOR GATE	28480	1820-0235
A3U22	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A3U23	1820-0272		INTEGRATED CIRCUIT:DIGITAL	04713	SC 7022PK
A4	01930-66504	1	BOARD ASSY:PROGRAM	28480	01930-66504
A4C1	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A4C2	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A4C3	0150-0093		C:FXD CER 0.01 UF +80-20% 100VDCW	91418	TA
A4C4	0180-2203		C:FXD ELECT 1.0 UF 20% 35VDCW	37942	TIM105M035POW
A4CR1	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR2	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR3	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR4	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR5	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR6	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR7	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR8	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR9	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR10	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR11	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR12	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR13	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR14	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR15	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR16	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR17	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR18	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR19	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR20	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR21	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR22	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR23	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR24	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR25	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR26	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR27	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR28	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR29	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR30	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR31	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR32	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR33	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR34	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR35	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR36	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR37	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR38	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR39	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR40	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR41	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR42	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR43	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR44	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR45	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR46	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR47	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR48	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR49	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR50	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR51	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR52	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR53	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR54	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR55	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR56	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A4CR57	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4L1	9100-2258	2	COIL/CHOKE 1.20UH 10%	28480	9100-2258
A4L2	9100-2258		COIL/CHOKE 1.20UH 10%	28480	9100-2258
A4Q1	1853-0036		TSTR:SI PNP	80131	2N3906
A4Q2	1854-0215		TSTR:SI NPN	80131	2N3904
A4Q3	1853-0036		TSTR:SI PNP	80131	2N3906
A4Q4	1853-0036		TSTR:SI PNP	80131	2N3906
A4R1	0684-1831	23	R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R2	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R3	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R4	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R5	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R6	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R7	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R8	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R9	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R10	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R11	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R12	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R13	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R14	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R15	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R16	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R17	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R18	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R19	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R20	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R21	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R22	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R23	0684-1831		R:FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A4R24	0684-3921	1	R:FXD COMP 3900 OHM 10% 1/4W	01121	CB 3921
A4R25	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R26	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R27	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R28	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R29	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R30	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R31	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R32	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R33	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R34	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R35	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R36	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R37	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R38	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R39	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R40	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R41	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R42	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R43	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R44	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R45	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R46	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R47	0684-4721		R:FXD COMP 4700 OHM 10% 1/4W	01121	CB 4721
A4R48	0684-1021		R:FXD COMP 1000 OHM 10% 1/4W	01121	CB 1021
A4R49	0684-3321	23	R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R50	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R51	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R52	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R53	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R54	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R55	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R56	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R57	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R58	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R59	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R60	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R61	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R62	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R63	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R64	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R65	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R66	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R67	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R68	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R69	0684-3321		R:FXD COMP 3300 OHM 10% 1/4W	01121	CB 3321

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A4R70	0684-3321		R:FXD CCMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R71	0684-3321		R:FXD CCMP 3300 OHM 10% 1/4W	01121	CB 3321
A4R72	0684-6811	1	R:FXD CCMP 680 OHM 10% 1/4W	01121	CB 6811
A4R73	0684-5621		R:FXD CCMP 5.6K OHM 10% 1/4W	01121	CB 5621
A4R74	0684-3311	1	R:FXD CCMP 330 OHM 10% 1/4W	01121	CB 3311
A4R75	0684-5621		R:FXD CCMP 5.6K OHM 10% 1/4W	01121	CB 5621
A4R76	0684-5611	2	R:FXD CCMP 560 OHM 10% 1/4W	01121	CB 5611
A4R77	0684-2231		R:FXD CCMP 22K OHM 10% 1/4W	01121	CB 2231
A4T81	01930-26504	1	BOARD:BLANK PC	28480	01930-26504
A4W1	01930-61601	2	CABLE ASSY:PROGRAMMING	28480	01930-61601
A5	01930-60001	1	DECK AND CABLE ASSY	28480	01930-60001
A5J1	1251-0233	4	CONNECTOR:PC 44 CONTACTS	28480	1251-0233
A5J2	1251-0233		CONNECTOR:PC 44 CONTACTS	28480	1251-0233
A5J3	1251-0233		CONNECTOR:PC 44 CONTACTS	28480	1251-0233
A5J4	1251-0233		CONNECTOR:PC 44 CONTACTS	28480	1251-0233
A5A1	01930-60101	1	DECK ASSY:MAIN	28480	01930-60101
A5A1MP1	01930-00101	1	DECK:MAIN	28480	01930-00101
A5A1T81	01930-26505	1	BOARD:BLANK PC	28480	01930-26505
A5Q1	1854-0072	1	TSTR:SI NPN	80131	2N3054
A6	01930-60002	1	SWITCH ASSY:WIRED	28480	01930-60002
A6MP1	01930-01202	1	BRACKET:SWITCH	28480	01930-01202
A6S1	3101-0070	2	SWITCH:SLIDE	79727	G-126
A6S2	3101-0070		SWITCH:SLIDE	79727	G-126
			CHASSIS PARTS		
H1	1390-0160	1	FASTENER:PANEL ASSY	08524	DHP-7500-10-C-5
J1	1250-0001	5	CONNECTOR:RF BNC BULKHEAD MOUNT JACK	28480	1250-0001
J2	1250-0001		CONNECTOR:RF BNC BULKHEAD MOUNT JACK	28480	1250-0001
J3	1250-0001		CONNECTOR:RF BNC BULKHEAD MOUNT JACK	28480	1250-0001
J4	1250-0001		CONNECTOR:RF BNC BULKHEAD MOUNT JACK	28480	1250-0001
J5	1250-0001		CONNECTOR:RF BNC BULKHEAD MOUNT JACK	28480	1250-0001
MP1	01930-00504	1	GUSSET:RIGHT SIDE	28480	01930-00504
MP2	01930-00505	1	GUSSET:LEFT SIDE	28480	01930-00505
MP3	01930-01204	1	BRACKET:CONNECTOR 1/4" MOD	28480	01930-01204
MP4	01930-00201	1	PANEL:FRONT	28480	01930-00201
MP5	01930-20201	1	FRAME:PANEL	28480	01930-20201
MP6	01930-64101	1	COVER ASSY:TOP	28480	01930-64101
MP7	01930-67401	1	KNOB	28480	01930-67401
MP8	1450-0731	1	CAP:LENS, GREEN	03797	HL230GT
P1	1251-2090	1	CONNECTOR:PC 15 PIN MALE ADAPTER	95354	189-194-168
P2	1251-0483	1	CONNECTOR:R & P MALE 36 CONTACT PLUG	28480	1251-0483
R39	0684-5611		R:FXD CCMP 560 OHM 10% 1/4W	01121	CB 5611
S1	3100-2686	1	SWITCH:ROTARY 2 SECTION 12 POS.	28480	3100-2686
S1	1450-0730	1	LAMPHOLDER ASSY:FRONT MTG. TYPE	03797	HLA1010
S2	3101-0163	2	SWITCH:TOGGLE SPDT	04009	MST-105D
S3	3101-1221	2	SWITCH:PUSHBUTTON SPDT	09353	P8121PC-3
S4	3101-0963	1	SWITCH:TOGGLE SPDT 5A 115V AC	95146	MST-105E
S5	3101-0163		SWITCH:TOGGLE SPDT	04009	MST-105D
S6	3101-1221		SWITCH:PUSHBUTTON SPDT	09353	P8121PC-3
W1	01930-61601		CABLE ASSY:PROGRAMMING	28480	01930-61601

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	ALLEN BRADLEY CO.	MILWAUKEE, WIS.	53204
03797	ELDEMA CORP.	COMPTON, CALIF.	90220
04009	ARROW, HART & HEGEMAN ELECT. CO.	HARTFORD, CONN.	06106
04713	MOTOROLA SEMICONDUCTOR PROD.INC.	PHOENIX, ARIZ.	85008
07263	FAIRCHILD CAMERA & INST. CORP. SEMICONDUCTOR DIV.	MOUNTAIN VIEW, CALIF.	94040
08524	DEUTSCH FASTENER CORP.	LOS ANGELES, CALIF.	90061
09353	C & K COMPONENTS INC.	NEWTON, MASS.	02158
28480	HEWLETT-PACKARD COMPANY	PALO ALTO, CALIF.	94304
36196	STANWYCK COIL PROD. LTD.	HAWKSBURY ONTARIO, CANADA	
37942	P. R. Mallory & CO., INC.	INDIANAPOLIS, IND.	
72982	ERIE TECHNOLOGICAL PROD. INC.	ERIE, PA.	16512
79727	CONTINENTAL-WIRT ELECTRONICS CORP.	PHILADELPHIA, PA.	19144
80131	ELECTRONIC INDUSTRIES ASSOCIATION	WASHINGTON D.C.	20006
91418	RADIO MATERIALS CO.	CHICAGO, ILL.	60646
95146	ALCO ELECT. PROD. INC.	LAWRENCE, MASS.	01843
95354	METHODE MFG. CO.	ROLLING MEADOWS, ILL.	60008
99800	DELEVAN ELECTRONICS CORP.	E. AURORA, N.Y.	14052

SECTION VII

MANUAL CHANGES AND OPTIONS

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument. Descriptions of special options and standard options are also in this section.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having a serial prefix as shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, refer to Table 7-1 for changes necessary to backdate the manual to the instrument. When making changes from Table 7-1, make the change with the highest number first. If the serial prefix of the instrument is not listed either in the title page or in Table 7-1, refer to an enclosed MANUAL CHANGES sheet for updating information. Also, if a MANUAL CHANGES sheet is supplied, make all indicated ERRATA corrections.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
No backdating changes are required at this time.	

7-5. SPECIAL OPTIONS.

7-6. Most customer special application requirements and/or specifications can be met by factory modification of a standard instrument. A standard instrument modified in this way will carry a special option number, such as Model 0000A/Option C01.

7-7. An operating and service manual and a manual insert are provided with each special option instrument. The operating and service manual contains information about the standard instrument. The manual insert for the special option describes the factory modifications required to produce the special option instrument. Amend the operating and service manual by changing it to include all manual insert information (and MANUAL CHANGES sheet information, if applicable). When these changes are made, the operating and service manual will apply to the special option instrument.

7-8. If you have ordered a special option instrument and the manual insert is missing, notify the nearest Hewlett-Packard Sales/Service Office. Be sure to give a full description of the instrument, including the complete serial number and special option number.

7-9. STANDARD OPTIONS.

7-10. Standard options are modifications installed on HP instruments at the factory and are available on request. Contact the nearest Hewlett-Packard Sales/Service Office for information concerning standard options.

SECTION VIII

SCHEMATICS AND TROUBLESHOOTING

8-1. INTRODUCTION.

8-2. This section contains schematics, repair and replacement information, component-identification illustration, waveforms, test conditions, troubleshooting charts and procedures. Figure 8-1 provides a guide to locating possible problems. Table 8-1 defines symbols and conventions used on the schematics. A disassembly procedure for removing boards A1 through A4 for repair and replacement is also contained in this section.

8-3. SCHEMATICS.

8-4. Schematics are printed on fold-out pages for easy reference to the text and figures in other sections. The schematics are drawn to show the electronic function of the circuits. Any one schematic may include all or part of several different physical assemblies.

8-5. The schematics are numbered in sequence with a bold number in a box at the lower right-hand corner of each page. These numbers are used to cross reference signal connections between schematics. At each circuit breaking point, a notation is made of the signal name and a number (in bold type). This number indicates the associated schematic which contains the source or destination of the signal. To find the source or destination of any point on a given schematic, turn to the schematic referred to by number and find the name of the signal in question.

8-6. A reference designations table on each schematic lists all components shown on the schematic. Component reference designators which have been deleted from the schematic are listed below the table.

8-7. All components within the shaded areas of a schematic are physically located on etched circuit boards. Components not physically located on an etched circuit board are shown in the unshaded areas of the schematic.

8-8. REFERENCE DESIGNATIONS.

8-9. The unit system of reference designations used in this manual is in accordance with the provisions of USA Standard Y32.16-1968, Reference Designations for Electrical and Electronics Parts and Equipments, dated March 1, 1968. Minor variations from the standard, due to design and manufacturing practices, may be noted.

8-10. Each electrical component is assigned a class letter and number. This letter-number combination is the basic reference designation. Components which are not part of an assembly have only the basic reference designation. Components which are part of an assembly have, in addition to the basic designation, a prefix designation indicating the assembly of which the component is a part (resistor R23 on assembly A1 is called A1R23).

8-11. Assemblies are numbered consecutively. If an assembly reference designation is assigned and later deleted, that number is not reused.

8-12. COMPONENT LOCATIONS.

8-13. Locations of components on assemblies and subassemblies are illustrated in photos adjacent to the schematics. Since the schematics are drawn to show function, portions of a particular assembly may appear on several different schematics. The component-location photo is printed next to the schematic that shows most of the circuitry on the assembly. Components located on the chassis are identified in Figure 8-2. The locations of all adjustments are shown in Section V.

8-14. REPAIR AND REPLACEMENT.

8-15. The following paragraphs provide procedures for removal and replacement of assemblies, subassemblies, and components in the Model 1930A. Special servicing instructions for the printed circuit boards are covered under Paragraph 8-27. Section VI provides a detailed parts list for use in ordering replacement parts.

8-16. SEMICONDUCTOR REPLACEMENT.

8-17. When removing a semiconductor, use long-nose pliers as a heat sink between the device and the soldering iron. When replacing a semiconductor, ensure sufficient lead length to dissipate the soldering heat by using the same length of exposed lead as was used for the original part.

8-18. CIRCUIT BOARD ASSEMBLY REMOVAL.

8-19. The plug-in circuit boards A1 through A4 must be removed for servicing. To remove the boards proceed as follows:

a. Remove screws holding connector bracket MP3 and drop bracket and connector downward.

b. Slide cover assembly MP6 to rear until it is free from lips of side gussets MP1 and MP2.

c. Grasp desired board at front and rear between thumbs and index fingers. Rock board gently forward and backward while exerting gentle pressure upwards until board is free of socket.

d. To re-install board, reverse above procedure.

Table 8-1. Schematic Notes

Refer to MIL-STD-15 1A for schematic symbols not listed in this table.

= Etched circuit board

= Front-panel marking

= Rear-panel marking

= Front-panel control

= Screwdriver adjustment

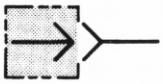
P/O = Part of

CW = Clockwise end of variable resistor

NC = No connection

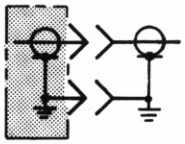
= Waveform test point (with number)

= Common electrical point (with letter) not necessarily ground

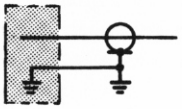


= Single-pin connector on board

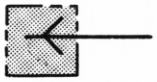
= Pin of a plug-in board (with letter or number)



= Coaxial cable connected to snap-on jack



= Coaxial cable connected directly to board



= Wire connected to pressure-fit socket on board

= Main signal path

= Primary feedback path

= Secondary feedback path

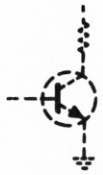
= Field-effect transistor (P-type base)

= Field-effect transistor (N-type base)

= Breakdown diode (voltage regulator)

= Tunnel diode

= Step-recovery diode

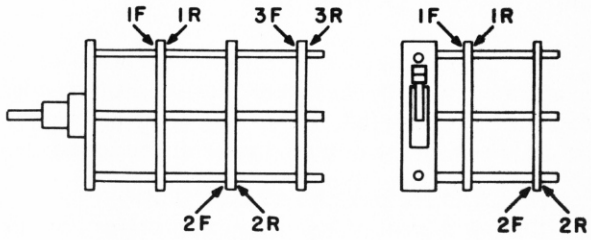


= Circuits or components drawn with dashed lines (phantom) show function only and are not intended to be complete. The circuit or component is shown in detail on another schematic.

(925) = Wire colors are given by numbers in parentheses using the resistor color code [(925) is wht-red-grn].

0 - Black	5 - Green
1 - Brown	6 - Blue
2 - Red	7 - Violet
3 - Orange	8 - Gray
4 - Yellow	9 - White

Switch wafers are identified as follows:



* = Optimum value selected at factory, typical value shown; part may have been omitted.

Unless otherwise indicated:
resistance in ohms
capacitance in picofarads
inductance in microhenries

8-20. CIRCUIT BOARDS.

8-21. The following paragraphs provide information regarding servicing procedures for etched circuit boards, use of heat sinks, and special soldering considerations.

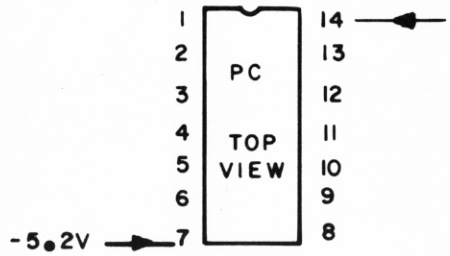
8-22. BOARD CONNECTIONS.

8-23. Wire connections are identified on circuit boards by the color code of the connecting wire. Connector pins on plugs and jacks are identified by a numeral or letter. The letters G, I, O, and Q have been omitted. Table 8-1 shows the types of board connections used in the instrument.

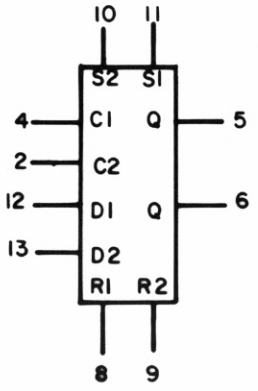
8-24. BOARD EXTENDER.

8-25. A plug-in board extender is provided. The extender may be used with any of the plug-in boards, permitting a circuit board to remain connected to the instrument, yet physically raised to a convenient level for circuit checks and adjustments. The board extender should not be used for making high frequency measurements (> 1 MHz).

Table 8-1. Schematic Notes, Continued



MECL. PIN CONNECTIONS



TYPE D FLIP-FLOP

LOGIC GATES

AND OR EXCLUSIVE NOR NOR OR/NOR

$\overline{K}$ = FEEDBACK TAP

$\overline{K}$, $\overline{DIV}$, ERROR ECT

A BAR OVER THE TOP OF A FUNCTION INDICATES THE COMPLEMENT OF THE FUNCTION

THE CABLES SHOWN AS COAXIAL CABLES ON THE SCHEMATICS ARE ACTUALLY SPECIALLY CONSTRUCTED TWISTED PAIR CABLES AND ARE REPLACEABLE WITH 50 Ω COAXIAL CABLE.

8-26. SERVICING ETCHED CIRCUIT BOARDS.

8-27. This instrument uses etched circuit boards with plated-through component holes. This allows components to be removed or replaced by unsoldering or soldering from either side of the board. When removing large components, such as potentiometers, rotate the soldering iron tip from lead to lead while applying pressure to the part to lift it from the board. HP Service Note M-20E contains additional information on the repair of etched circuit boards.

8-28. INTEGRATED CIRCUIT REPLACEMENT.

8-29. The IC (integrated circuits) in this instrument are soldered in place. Soldered IC units may be removed with soldering irons which simultaneously heat all connections (available from various manufactures). Soldering irons with built-in desoldering tools also facilitate quick removal.

CAUTION

Unless an IC has definitely failed, be careful to prevent damage when removing or replacing it.

8-30. Use the following procedure for removing an IC with a standard soldering iron.

a. Heat IC lead solder joint. Use soldering iron with small pencil tip (e. g. Weller No. PT-H7).

b. When solder is fluid, remove it with desoldering tool (such as deluxe model Soldapullt manufactured by Edsyn Company of California).

c. Repeat steps a and b for each IC lead until all leads are free.

d. Grasp each lead with long-nose pliers and check that it is mechanically free from circuit board.

e. When all leads are free, carefully remove IC, Dual in-line type may be removed by gently gripping top and bottom with long-nose pliers and rolling IC out.

f. Use desoldering tool or toothpick to remove all remaining solder from circuit board holes.

g. Insert replacement IC into circuit board and solder it in place.

CAUTION

Be careful not to damage the IC by heat from the soldering iron. Work quickly.

8-31. When replacing an IC, note the mark or notch used for orientation. The component identification photos and the IC pin-location diagrams in Table 8-1 show IC orientation.

8-32. TROUBLESHOOTING.

8-33. The most important prerequisites for successful troubleshooting are understanding how the instrument is designed to operate and correct use of front-panel controls. Suspected malfunctions may be caused by improper control settings or circuit connections. Before doing the test and/or troubleshooting procedures, read Section III (Operation) for an explanation of controls and connectors and general operating considerations, and Section IV (Principles of Operation) for an explanation of circuit theory.

8-34. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble. Check to see that all circuit board connections are making good contact and are not shorting to an adjacent circuit, If no obvious trouble is found, check the power supply voltages in the unit. Prior to any extensive troubleshooting, check the external power sources also. Figure 8-2 lists several of the most common malfunctions and probable sources of trouble.

8-35. DC VOLTAGES.

8-36. On some of the schematics, dc voltages are indicated for active components (transistors, etc). Conditions for making the voltage measurements are listed adjacent to each schematic. Since the conditions for making these measurements may differ from one circuit to another, always check the specific conditions listed adjacent to the schematic.

8-37. WAVEFORMS.

8-38. Waveform measurement points (▽ with a number enclosed) are placed on the schematics along main signal paths. The numbers inside the measurement point symbols (▽) are keyed to corresponding waveforms adjacent to each schematic. Conditions for making the waveform measurements are also listed adjacent to each schematic. Like the dc voltage measurement conditions, waveform measurement conditions may vary from one circuit to another.

8-39. CIRCUIT CHECKING.

8-40. To troubleshoot the Model 1930A proceed as follows:

a. Remove Model 1930A from 1900-series mainframe.

b. Set two interface switches on left side to the forward position.

c. Connect extender (HP 10484A) between Model 1930A and mainframe compartment connector.

NOTE

Make as many checks as possible from the connections on plugs A5P1-A5P4. If it is not possible to do this the board must be removed (refer to paragraph 8-18) and the plug-in board extender used.

8-41. In all but the simplest failures it is very difficult to troubleshoot the Model 1930A in DIVIDE or NORM. Use MULTIPLY as much as possible. In MULTIPLY, with no external data inputs applied, the Model 1930A will generate short repetitive words which are easy to trace thru the logic circuits. In the multiply mode the shift register will be loaded with all 0's. When the all 0 state is detected by the word detector, a 1 will be loaded into the flip-flop that drives the feed-forward line. On the next clock pulse, the 1 on the feed-forward line will be loaded into every shift register cell whose gate to the feed-forward line is on. These 1's will then be clocked out of the shift register in serial form and can be traced through all the control circuitry and shift register flip-flops. Refer to paragraph 4-38 for a complete explanation of this operation.

8-42. Try to find a pulsating signal and trace it through the logic circuitry until it comes to the input of some IC but does not make it to the output.

8-43. MECL swings are small and negative. Logic 1 is −0.7 volt and logic 0 is −1.5 volts. Threshold is −1.2 volts. An oscilloscope provides a convenient means of tracing and identifying logic levels. Set the oscilloscope up as follows:

INPUT	DC
Trigger Mode	Free run or auto
Vertical Sensitivity	Approximately 0.5 V/div.
Vertical Position	To place the 0 level (−1.5V) along X axis.
Sweep speed	Any convenient speed.

The trace, with no input, will be near the top of the graticule. A 0 will place the trace on the X axis and a 1 will place the trace slightly below the no signal level.

8-44. Most troubles can be localized by following the troubleshooting chart (Figure 8-1). Many checks on the chart are level measurements to determine if the level is more positive than −1.2 volts (logic 1) or more negative than −1.2 volts (logic 0).

8-45. Initial set-up for using the troubleshooting chart is as follows:

a. Install the Model 1930A in the 1900-series mainframe using the extender (HP Part No. 10484A) supplied with the mainframe.

b. Supply a 1 MHz clock pulse to CLOCK INPUT. If a Model 1905A or 1906A is used as a clock generator, it can be installed in the extender alongside the Model 1930A.

c. Set REGISTER LENGTH switch to PGM. Program multiply mode. Refer to Section III, starting at paragraph 3-70, for instructions for programing the Model 1930A.

d. If an external programer is available, it should be used to expedite the test procedure. A simple programer can be fabricated using a SPST switch for each feedback tap and function (25 switches and the plug shown in Figure 3-8). Neither or these being available, the programing taps can be grounded by using short wire jumpers with small alligator clips on each end.

8-46. The wiring diagram (Figure 8-16) is useful to locate test points and trace signals.

Check mainframe power supplies

BAD

① Check input voltages
A5P1–13 +25V ±1%
A5P1–8 gnd
A5P1–10 –10V ±20%
A5P1–11 –25V ±1%

② Check power supply regulator
A5J2–A –5.2V ±.2

BAD

Check for short circuits or hot components.

BAD

Check voltage at base of A1Q3. <.4V

GOOD

Check for –5.8V on base of A1Q1. Check for bad A1Q1 or Q1.

Trace clock pulse from A5J1-A to base of A1Q4 to collector of A1Q7 to emitter of A1Q7 to A5J1,2, 3,5

BAD

③ Set bias to –1.8V. Ensure that $\overline{CL}$ is available at A5J1–2,3,5

Repair REGISTER LENGTH switch or wiring

BAD

Check collector of A4Q1 for +25V. Check emitter of A4Q3 for –4V. Check to see that A4CR 27/28/29 are reverse biased.

BAD

Check:
A4Q1 – A4Q4
A4R73 – A4R77
A4CR26 – A4CR29

GOOD

Check A5J4–4 for –5.2V

BAD

④ Ensure that front panel switches do not affect PRBS output and that $\overline{MULT}$ input to A5J1–17 is Logic "0"

Check MULT ckt.
A1Q12, A1Q13.
A1R26 – A1R30
A1C4

BAD

⑤ Check MULT line at A5J1–22 for Logic "1"

Check logic on A1U1 and A1U2

BAD

⑥ Check following levels on A5J1.
Pin 6 Logic "1"
Pin 7 $\overline{CL}$ pulses
Pin 8 Logic "0"
Pin 8 Logic "1"

Locate point of test on wiring diagram. Trace back to trouble.

BAD

⑦ Check following on A5J2:
Pin 1 Logic "1"
Pin B and Z $\overline{CL}$ pulses
pin 19 Logic "0"
Pin A –5.2V
Pin Y Logic "1"
Pin V Logic "1"

NOTES

1 Logic 1: more positive than –1.2V
Logic 0: more negative than –1.2V

2 Check with oscilloscope. Look for single square wave every N + 1 clock pulses. For example, if K2 is programmed, there will be 1 square wave every 3 clock pulses.

⑧ With all gates programed off, ensure that TRIGGER OUTPUT consists of square waves.

BAD

Check:
A2U19–13
A2U19–8,9
A2U22–9
A2U10–6
A2U10–2
Logic "0" NOTE 2

BAD

⑨ Program $\overline{K1}$. Ensure that both PRBS OUTPUT and TRIGGER OUTPUT are square waves.

Check:
A2U19–1
A2U19–5,6
A2U21–4
A2U9–6
Logic "0" NOTE 2

BAD

⑩ Open $\overline{K1}$ and program $\overline{K2}$. Both TRIGGER and PRBS OUTPUTS should be pulses of period 3.

⑪

A2U14 or A2U15 bad

Logic "1"

Check level at A2U10–2

Logic "0"

A2U10 bad

Logic "1"

Check level at A2U10–10

Logic "0"

Broken printed circuit or open A2L5

Logic "0"

Check level at A5J2–C

Logic "1"

Ensure that each point on A2U14 pins 4,5,6,8,9,10 is "0"

BAD

Follow the input back to associated F/F to find which one is 1. Ensure that pin 6 on F/F is 1. If F/F output is 0, ensure that pin 13 (input) is 0. Trace back down the line until a F/F is found with 0 on both pins 6 and 13. This is the bad F/F. Before replacing it, ensure that it has a good clock pulse.

BAD

Check trigger A5J2–C Square wave

GOOD

Check for bad part in trigger amplifier, A1Q29 – A1Q32, A1R56. Check for square waves on A5J1–19. Ensure that output is terminated in 50 ohms.

race clock pulse from
5J1-A to base of A1Q4
collector of A1Q7 to
mitter of A1Q7 to A5J1,2, 3,5

BAD

3
Set bias to −1.8V.
Ensure that $\overline{CL}$ is
available at A5J1−2,3,5

Repair REGISTER
LENGTH switch or
wiring

Check collector of A4Q1 for
+25V. Check emitter of A4Q3
for −4V. Check to see that
A4CR 27/28/29 are reverse
biased.

BAD

Check:
A4Q1 − A4Q4
A4R73 − A4R77
A4CR26 − A4CR29

BAD GOOD

Check A5J4−4
for −5.2V

BAD

4
Ensure that front panel
switches do not affect
PRBS output and that
MULT input to A5J1−17
is Logic "0"

Check MULT ckt.
A1Q12, A1Q13.
A1R26 − A1R30
A1C4

BAD

5
Check MULT line
at A5J1−22 for Logic "1"

Check logic
on A1U1 and A1U2

BAD

6
Check following levels on
A5J1.
Pin 6 Logic "1"
Pin 7 $\overline{CL}$ pulses
Pin 8 Logic "0"
Pin 8 Logic "1"

Locate point of test on
wiring diagram. Trace
back to trouble.

BAD

7
Check following on A5J2:
Pin 1 Logic "1"
Pin B and Z $\overline{CL}$ pulses
pin 19 Logic "0"
Pin A −5.2V
Pin Y Logic "1"
Pin V Logic "1"

NOTES

1 Logic 1: more positive than −1.2V
Logic 0: more negative than −1.2V

2 Check with oscilloscope.
Look for single square wave
every N + 1 clock pulses. For
example, if K2 is programmed,
there will be 1 square wave every
3 clock pulses.

8
With all gates pro-
gramed off, ensure
that TRIGGER OUT-
PUT consists of
square waves.

BAD

Check:
A2U19−13
A2U19−8,9
A2U22−9
A2U10−6
A2U10−2
} Logic "0" NOTE 2

BAD

9
Program $\overline{K1}$. Ensure
that both PRBS OUT-
PUT and TRIGGER
OUTPUT are square
waves.

Check:
A2U19−1
A2U19−5,6
A2U21−4
A2U9−6
} Logic "0" NOTE 2

BAD

10
Open $\overline{K1}$ and program
$\overline{K2}$. Both TRIGGER and
PRBS OUTPUTS should
be pulses of period 3.

Check A2U11, then
check A2U24−1,2,3.

11
Open $\overline{K2}$ and close
(program) $\overline{K3}$. Both
TRIGGER and PRBS
OUTPUTS should be
pulses of period 4.

BAD

Check A1U3

GOOD

Check for pattern
at A5J1−18

BAD

GOOD

Check MULT
line on A1
for Logic "0"

BAD

Ensure level at
A5J1−22 is Logic "0"

12
Continue in this fashion
until all gates 1 through
20 have been checked. If
a gate will not work, leave
it closed and close the pre-
vious gate. This will provide
a signal for tracing with an
oscilloscope.

BAD

13
Open multiply line.
Program $\overline{K3}$ and $\overline{K5}$.
PRBS output should
be a repetitive pattern
31 bits long.

GOOD

Check other front
panel sequences as
desired

GOOD

FINISH
Instrument OK

A2U14 or A2U15
bad

Logic "1"

Check level at
A2U10−2

Logic "1"

Check level at
A2U10−10

Logic "0"

Broken printed
circuit or open
A2L5

Logic "0"

A2U10 bad

Logic "0"

Check level at
A5J2−C

BAD

Check trigger
A5J2−C
Square wave

GOOD

Check for bad part in trigger amplifier,
A1Q29 − A1Q32, A1R56. Check for
square waves on A5J1−19. Ensure that
output is terminated in 50 ohms.

Logic "1"

Ensure that each
point on A2U14
pins 4,5,6,8,9,10
is "0"

BAD

Follow the input back to associated F/F to find which one
is 1. Ensure that pin 6 on F/F is 1. If F/F output is 0, ensure
that pin 13 (input) is 0. Trace back down the line until a F/F
is found with 0 on both pins 6 and 13. This is the bad F/F.
Before replacing it, ensure that it has a good clock pulse.

Check:
A2U18−9
A2U18−8
A2U20−12
A2U8−13
A2U8−6
} Logic "0" NOTE 2

1930A-D-8

Figure 8-1.
Troubleshooting Chart

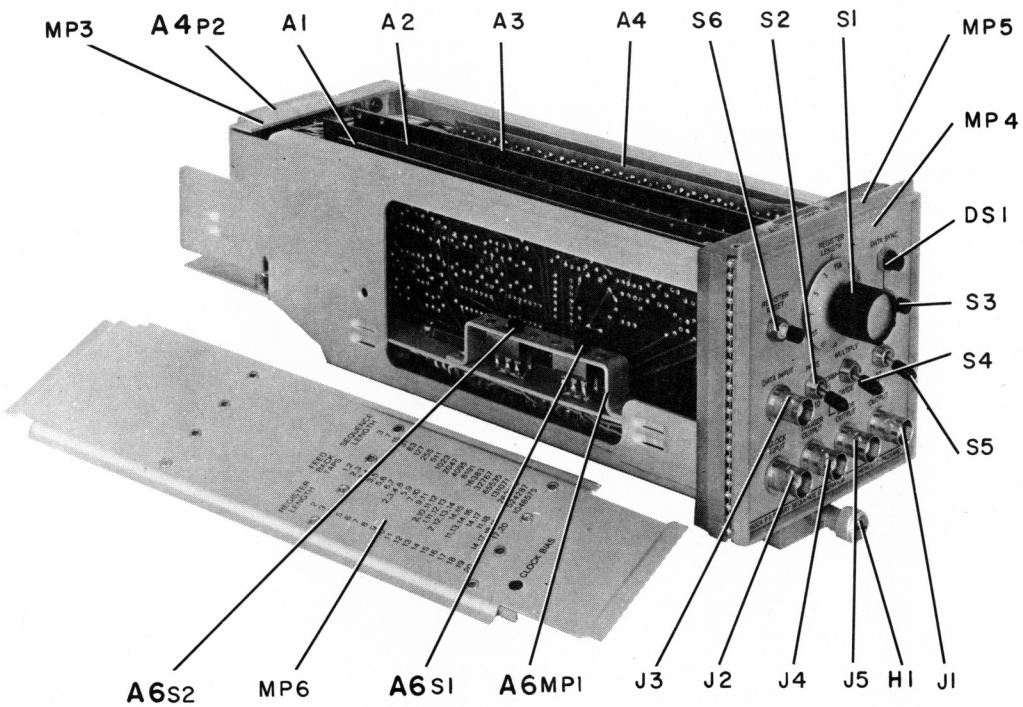


Figure 8-2. Chassis Parts Identification

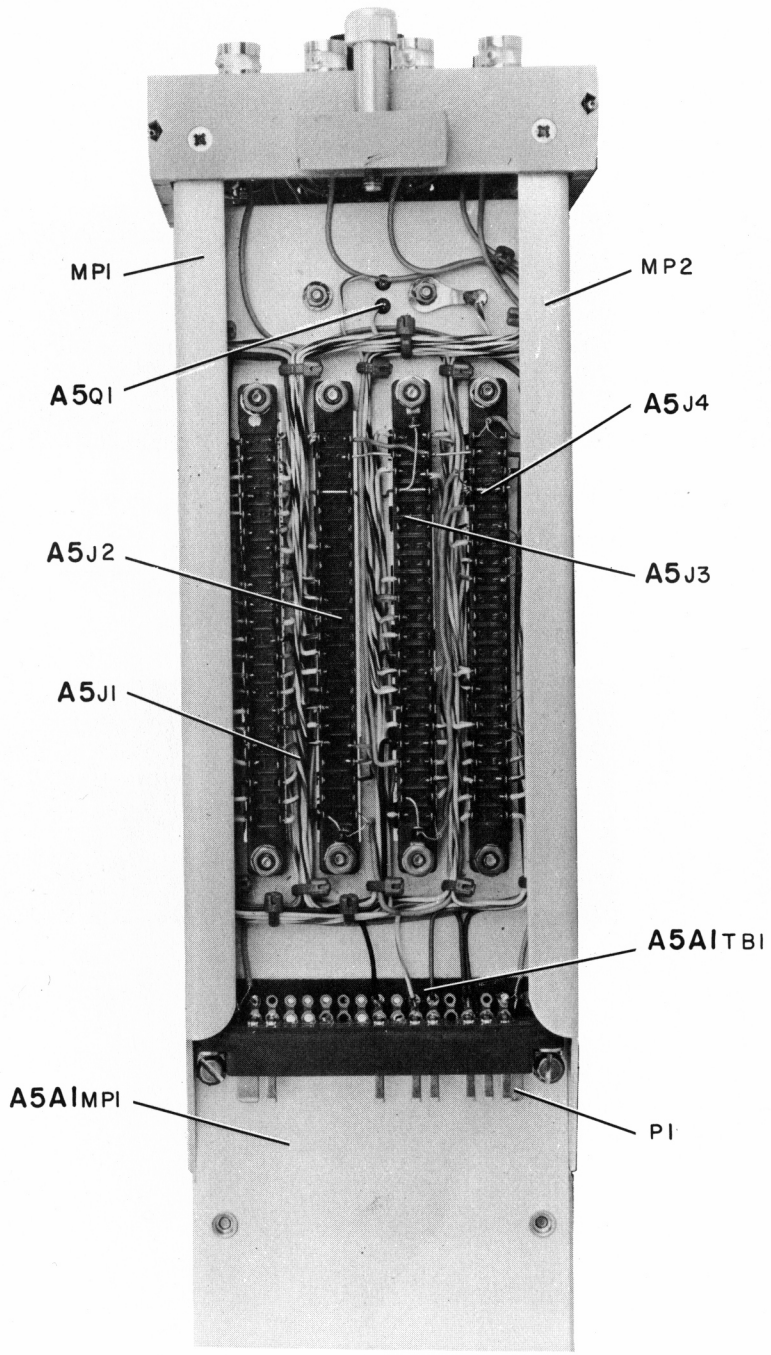
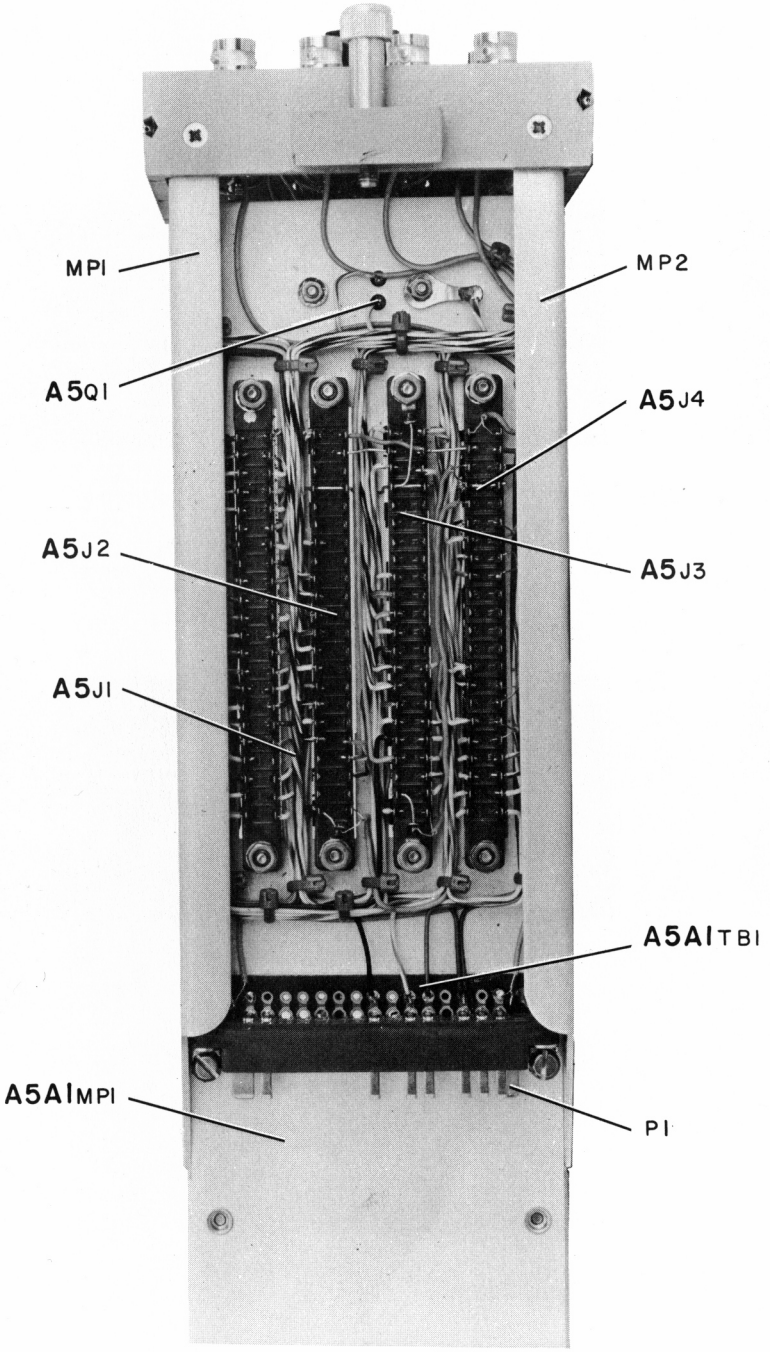
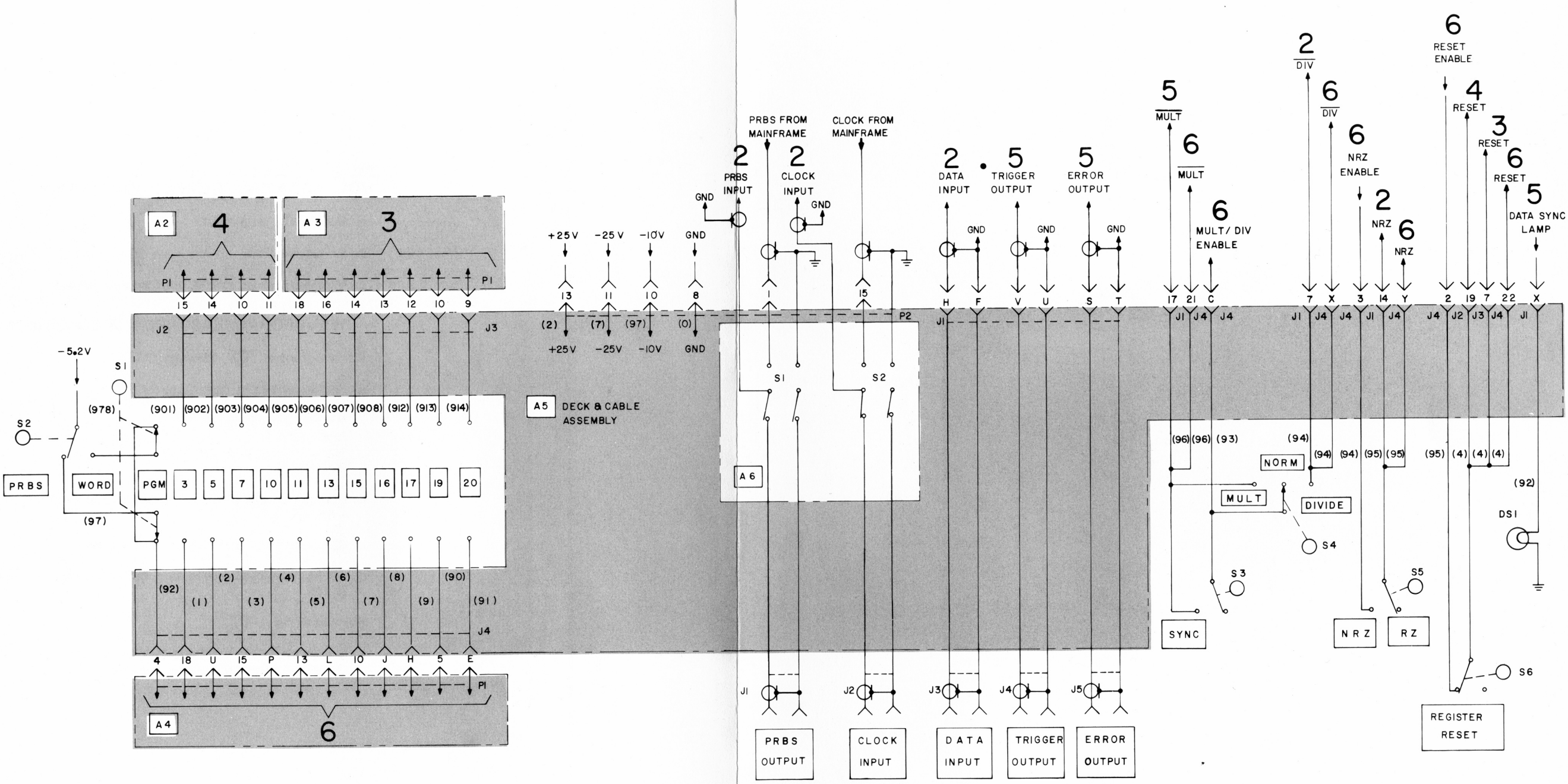


Figure 8-3. Assembly A5 Component Identification


MP1
MP2
A5Q1
A5J4
A5J2
A5J3
A5J1
A5A1TB1
A5A1MP1
P1



1930A—INPUT/OUTPUT SW.—987
1930A-D-5

A5	CHASSIS	A6
J1-4	DS-1 J1-5 S1-6 P1	S1-6

DELETED:

1

Figure 8-4.
Input, Output and Switching Schematic

VOLTAGE MEASUREMENT CONDITIONS

a. No clock or data input.

b. Switch positions . . . . . any

c. Voltages may vary ±20% between instruments.

WAVEFORM MEASUREMENT CONDITIONS

1. For waveforms ▽1 through ▽6

   a. Set Model 1930A controls as follows:

   REGISTER LENGTH 6
   PRBS/WORD . . . . . WORD
   MULTIPLY/NORM/DIVIDE . . . . . DIVIDE
   RZ/NRZ. . . . . NRZ

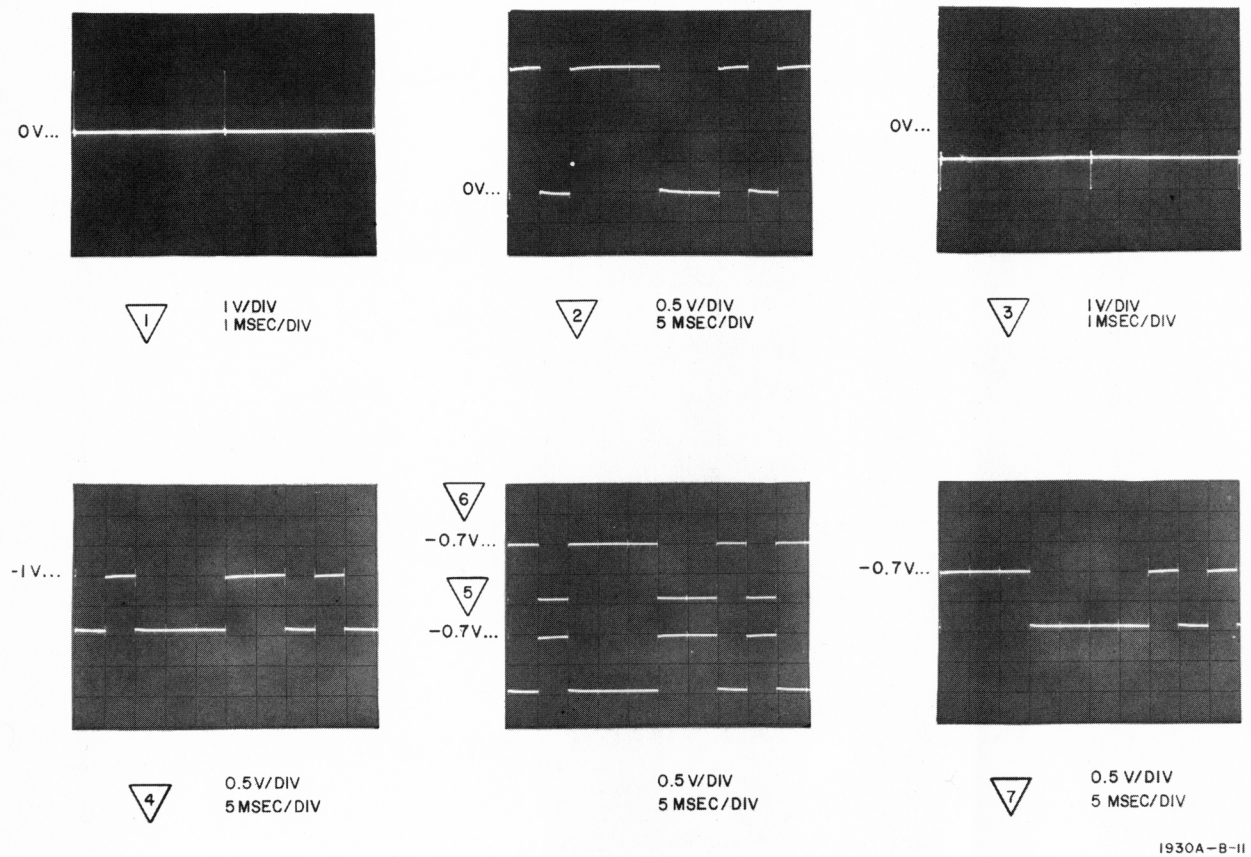
   b. Connect output of clock generator (200 kHz) to CLOCK INPUT.

   c. Connect PRBS OUTPUT to DATA INPUT.

   d. Set Monitor oscilloscope as noted below each waveform photo.

2. For waveform ▽7

   a. Switch MULTIPLY/NORM/DIVIDE switch to MULTIPLY. Other conditions same as in paragraph 1 above.



▽1 1 V/DIV, 1 MSEC/DIV

▽2 0.5 V/DIV, 5 MSEC/DIV

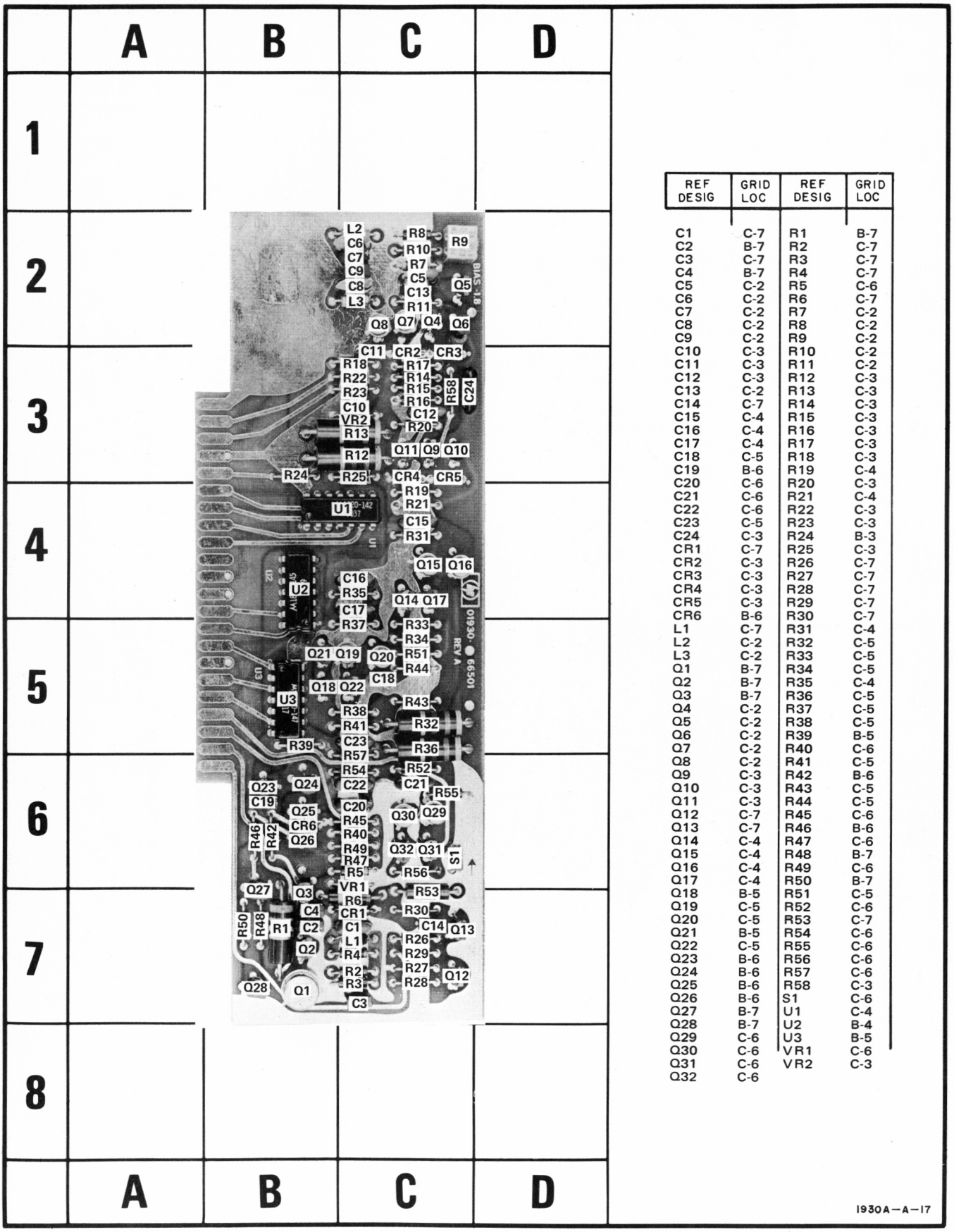
▽3 1 V/DIV, 1 MSEC/DIV

▽4 0.5 V/DIV, 5 MSEC/DIV

0.5 V/DIV, 5 MSEC/DIV

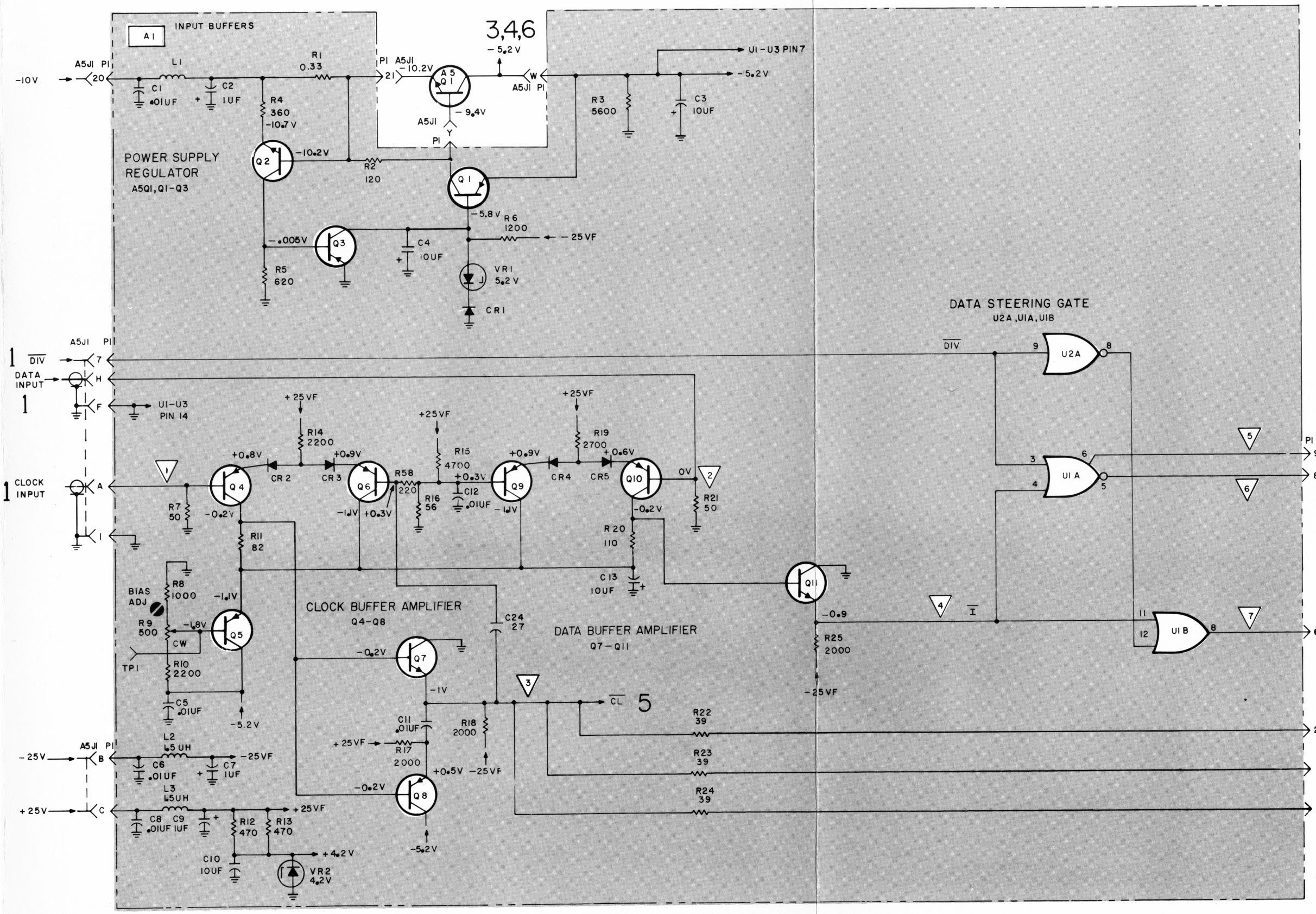
▽7 0.5 V/DIV, 5 MSEC/DIV

Figure 8-5. Voltage and Waveform Conditions for Schematic 2



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-7	R1	B-7
C2	B-7	R2	C-7
C3	C-7	R3	C-7
C4	B-7	R4	C-7
C5	C-2	R5	C-6
C6	C-2	R6	C-7
C7	C-2	R7	C-2
C8	C-2	R8	C-2
C9	C-2	R9	C-2
C10	C-3	R10	C-2
C11	C-3	R11	C-2
C12	C-3	R12	C-3
C13	C-2	R13	C-3
C14	C-7	R14	C-3
C15	C-4	R15	C-3
C16	C-4	R16	C-3
C17	C-4	R17	C-3
C18	C-5	R18	C-3
C19	B-6	R19	C-4
C20	C-6	R20	C-3
C21	C-6	R21	C-4
C22	C-6	R22	C-3
C23	C-5	R23	C-3
C24	C-3	R24	B-3
CR1	C-7	R25	C-3
CR2	C-3	R26	C-7
CR3	C-3	R27	C-7
CR4	C-3	R28	C-7
CR5	C-3	R29	C-7
CR6	B-6	R30	C-7
L1	C-7	R31	C-4
L2	C-2	R32	C-5
L3	C-2	R33	C-5
Q1	B-7	R34	C-5
Q2	B-7	R35	C-4
Q3	B-7	R36	C-5
Q4	C-2	R37	C-5
Q5	C-2	R38	C-5
Q6	C-2	R39	B-5
Q7	C-2	R40	C-6
Q8	C-2	R41	C-5
Q9	C-3	R42	B-6
Q10	C-3	R43	C-5
Q11	C-3	R44	C-5
Q12	C-7	R45	C-6
Q13	C-7	R46	B-6
Q14	C-4	R47	C-6
Q15	C-4	R48	B-7
Q16	C-4	R49	C-6
Q17	C-4	R50	B-7
Q18	B-5	R51	C-5
Q19	C-5	R52	C-6
Q20	C-5	R53	C-7
Q21	B-5	R54	C-6
Q22	C-5	R55	C-6
Q23	B-6	R56	C-6
Q24	B-6	R57	C-6
Q25	B-6	R58	C-3
Q26	B-6	S1	C-6
Q27	B-7	U1	C-4
Q28	B-7	U2	B-4
Q29	C-6	U3	B-5
Q30	C-6	VR1	C-6
Q31	C-6	VR2	C-3
Q32	C-6		

Figure 8-6. Board Assembly A1 Component Identification

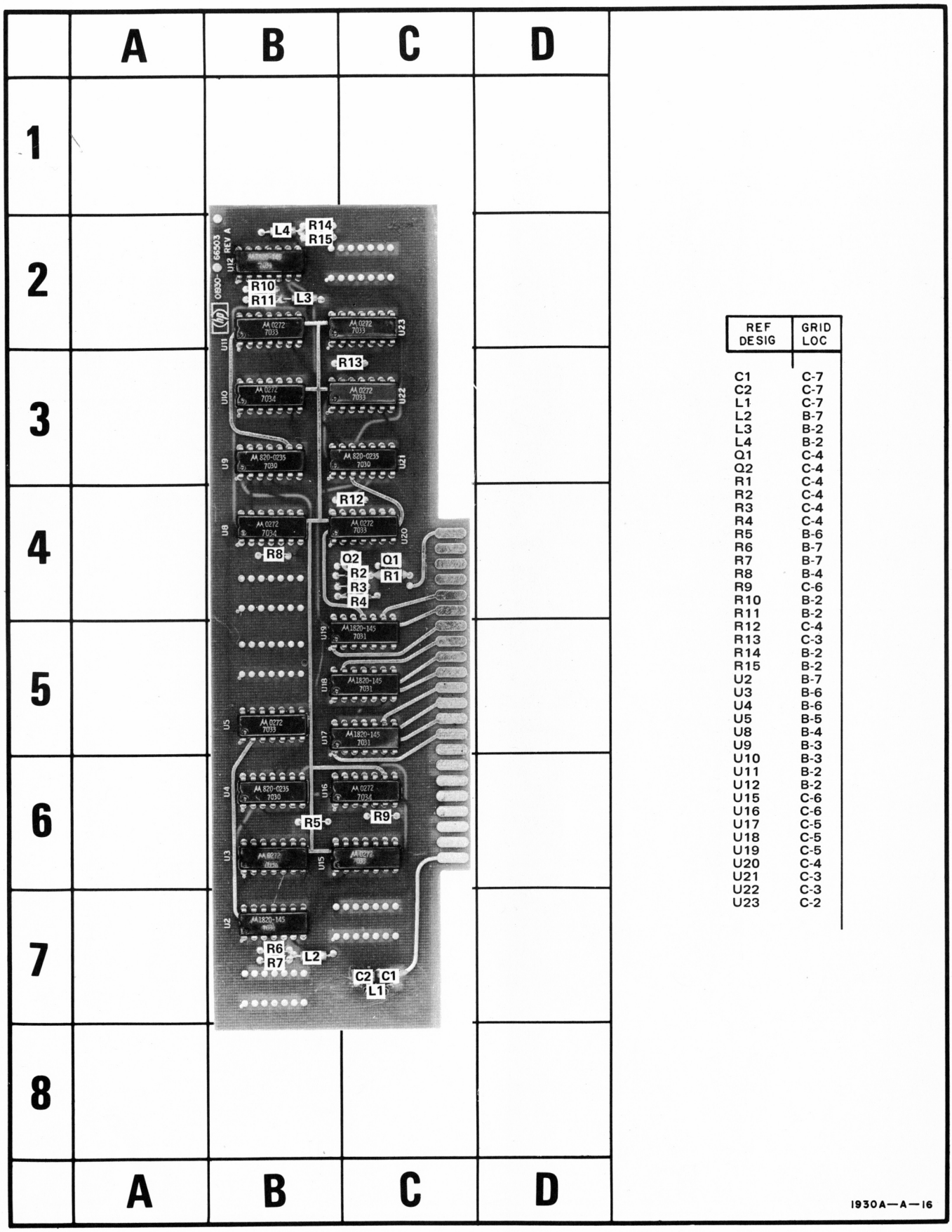


REFERENCE DESIGNATIONS

A1	A5
U1, P/O, U2 C1-C13, C24 CR1-CR5 L1-L3 Q1-Q11 R1-R25, R58 VR1-VR2	Q1 P/O J1

2

Figure 8-7.
Input Buffers Schematic



REF DESIG	GRID LOC
C1	C-7
C2	C-7
L1	C-7
L2	B-7
L3	B-2
L4	B-2
Q1	C-4
Q2	C-4
R1	C-4
R2	C-4
R3	C-4
R4	C-4
R5	B-6
R6	B-7
R7	B-7
R8	B-4
R9	C-6
R10	B-2
R11	B-2
R12	C-4
R13	C-3
R14	B-2
R15	B-2
U2	B-7
U3	B-6
U4	B-6
U5	B-5
U8	B-4
U9	B-3
U10	B-3
U11	B-2
U12	B-2
U15	C-6
U16	C-6
U17	C-5
U18	C-5
U19	C-5
U20	C-4
U21	C-3
U22	C-3
U23	C-2

Figure 8-8. Board Assembly A3 Component Identification

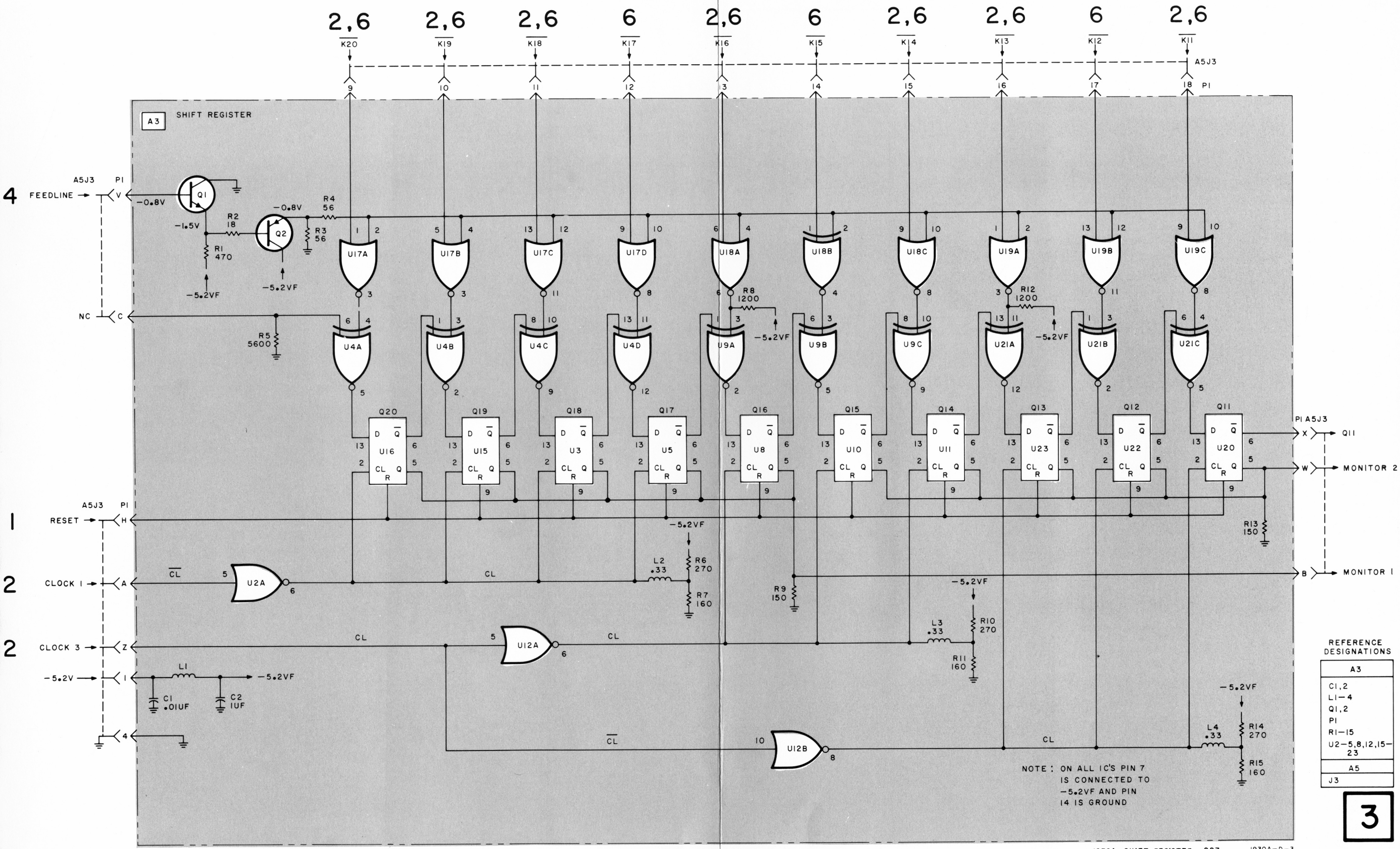
VOLTAGE MEASUREMENT CONDITIONS

a. No clock or data input.

b. Switch positions . . . . . any

c. Voltages may vary ±20% between instruments.

Figure 8-9. Voltage and Waveform Conditions for Schematic 3

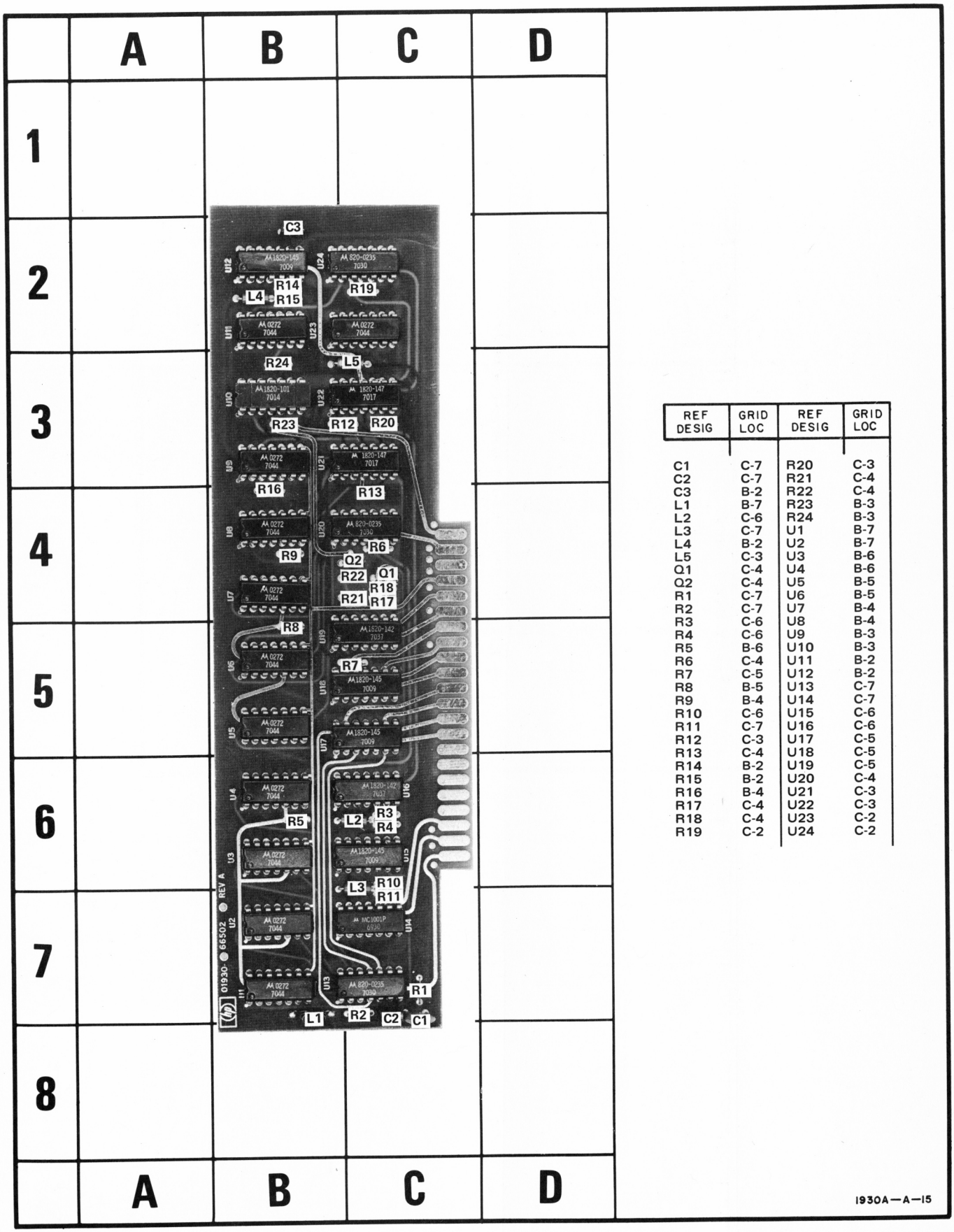


REFERENCE DESIGNATIONS

A3
C1,2 L1−4 Q1,2 P1 R1−15 U2−5,8,12,15−23
A5
J3

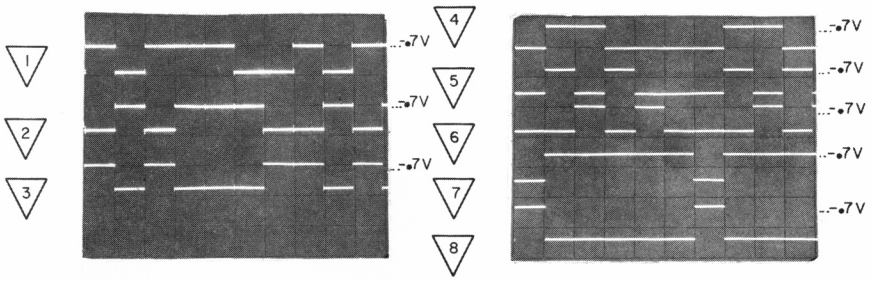
3

Figure 8-10.
Shift Register Schematic



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	C-7	R20	C-3
C2	C-7	R21	C-4
C3	B-2	R22	C-4
L1	B-7	R23	B-3
L2	C-6	R24	B-3
L3	C-7	U1	B-7
L4	B-2	U2	B-7
L5	C-3	U3	B-6
Q1	C-4	U4	B-6
Q2	C-4	U5	B-5
R1	C-7	U6	B-5
R2	C-7	U7	B-4
R3	C-6	U8	B-4
R4	C-6	U9	B-3
R5	B-6	U10	B-3
R6	C-4	U11	B-2
R7	C-5	U12	B-2
R8	B-5	U13	C-7
R9	B-4	U14	C-7
R10	C-6	U15	C-6
R11	C-7	U16	C-6
R12	C-3	U17	C-5
R13	C-4	U18	C-5
R14	B-2	U19	C-5
R15	B-2	U20	C-4
R16	B-4	U21	C-3
R17	C-4	U22	C-3
R18	C-4	U23	C-2
R19	C-2	U24	C-2

Figure 8-11. Board Assembly A2 Component Identification



VOLTAGE MEASUREMENT CONDITIONS

a. No clock or data input.

b. Switch positions . . . . . any

c. Voltages may vary ±20% between instruments.

WAVEFORM MEASUREMENT CONDITIONS

1. For waveforms ▽1 , ▽2 , and ▽3

   a. Set Model 1930A controls as follows:

      REGISTER LENGTH 3
      PRBS/WORD . . . . . WORD
      MULTIPLY/NORM/DIVIDE . . . . . DIVIDE
      RZ/NRZ . . . . . NRZ

   b. Connect output of clock generator (200 kHz) to CLOCK INPUT.

   c. Connect PRBS OUTPUT to DATA INPUT.

   d. Set monitor oscilloscope as noted below each waveform photo.

2. For waveforms ▽4 through ▽8 .

   a. Set Model 1930A controls as follows:

      REGISTER LENGTH 5
      PRBS/WORD . . . . . WORD
      MULTIPLY/NORM/DIVIDE . . . . . MULTIPLY
      RZ/NRZ . . . . . NRZ

   b. Disconnect PRBS OUTPUT from DATA INPUT.

Figure 8-12. Voltage and Waveform Conditions for Schematic 4

A2

CLOCK INPUTS AND SHIFT REGISTER

2,6 $\overline{K10}$ · 6 $\overline{K9}$ · 6 $\overline{K8}$ · 2,6 $\overline{K7}$ · 6 $\overline{K6}$ · 2,6 $\overline{K5}$ · 6 $\overline{K4}$ · 2,6 $\overline{K3}$ · 2 ID · 6 $\overline{K2}$ · 6 $\overline{K1}$ · 3 MONITOR 2 · 3 MONITOR 1

A5J2 P1

U17A U17B U17C U17D U18A U18B U18C U18D U19A P1 U19B

R2 1200 · R6 1200 · R7 1200 · R19 1200

U13A U13B U13C U13D U20A U20B U20C U20D

Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1

U1 U2 U3 U4 U5 U6 U7 U8 U9 U10

R1 5600

MONITOR 3 · MONITOR 4

-5.2V R5 180 · L2 0.33 · R3 270 · R4 160

R8 270 · R9 1200 · L3 0.33 · R10 270 · R11 160

U15A U15B

R12 56 · R20 56

DIVIDE GATE
U21A-U21C/U22A

U21A U21B U21C U22A

R13 470 · R16 1200

MULTIPLY GATE
U22B/U22C/U12B/U12C

U22B U22C

R17 56 · R18 56 · Q1 · -0.7V · -1.5V · R21 18 · R22 470 · Q2 · -0.8V · -5.2V · -5.2V · R23 56

WORD DET
U14/U15C/U15

FROM MONITOR 3 · FROM MONITOR 4 · MONITOR 5 · MONITOR 6 · MONITOR 7

U14 U16A

WAVE FORMS ARE TAKEN ON MONITORS 4,5, AND 6

RESET 1 · CLOCK 2 · $\overline{ID}$ 2 · MULT 2 · $\overline{IM}$ 2 · -5.2V 2 · GND · CLOCK 2 2

L1 · C1 .01UF · C2 1UF · C3 1UF

NOTE: ON ALL IC'S PIN 7 IS CONNECTED TO -5.2V AND PIN 14 IS GROUND.

MULT · $\overline{IM}$

U12A U12B U12C

L5 1

DATA COMPARATOR
U24A/U24B

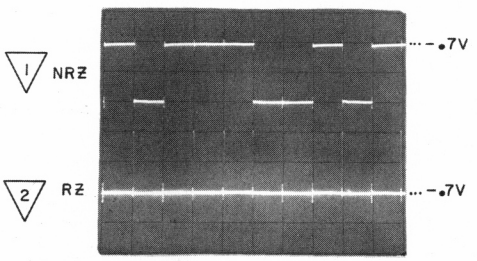
U24A U24B

-5.2V R14 270 · L4 0.33 · R15 160

U11 U23

R24 56

1930A— CLOCK INPUT



VOLTAGE MEASUREMENT CONDITIONS

a. No clock or data input.

b. Switch positions . . . . . any

c. Voltages may vary ±20% between instruments.

WAVEFORM MEASUREMENT CONDITIONS

1. For waveform 1

   a. Set Model 1930A controls as follows:

      REGISTER LENGTH 3
      PRBS/WORD . . . . . WORD
      MULTIPLY/NORM/DIVIDE . . . . . DIVIDE
      RZ/NRZ. . . . . NRZ

   b. Connect output of clock generator (200 kHz) to CLOCK INPUT.

   c. Connect PRBS OUTPUT to DATA INPUT.

   d. Set monitor oscilloscope as noted below waveform photo.

2. For waveform 2

   a. Switch RZ/NRZ switch to RZ. All other conditions same as in paragraph 1 above.

Figure 8-14. Voltage and Waveform Conditions for Schematic 5

P/O A1 OUTPUT BUFFERS

MULTIPLY ENABLE GATE
Q12/Q13

PRBS BUFFER AMPLIFIER
Q14-Q17

OUTPUT GATE
U3A, U3B, U3C

RZ/NRZ GATE
U2B/U2C/U2D

ERROR BUFFER AMPLIFIER
Q18-Q22

SYNC INDICATOR
Q23-Q28

TRIGGER BUFFER AMPLIFIER
Q29-Q32

REFERENCE DESIGNATIONS

A1
P/O U2/U3 C14 - C23 CR6- Q12 - Q32 R26 - R57 S1

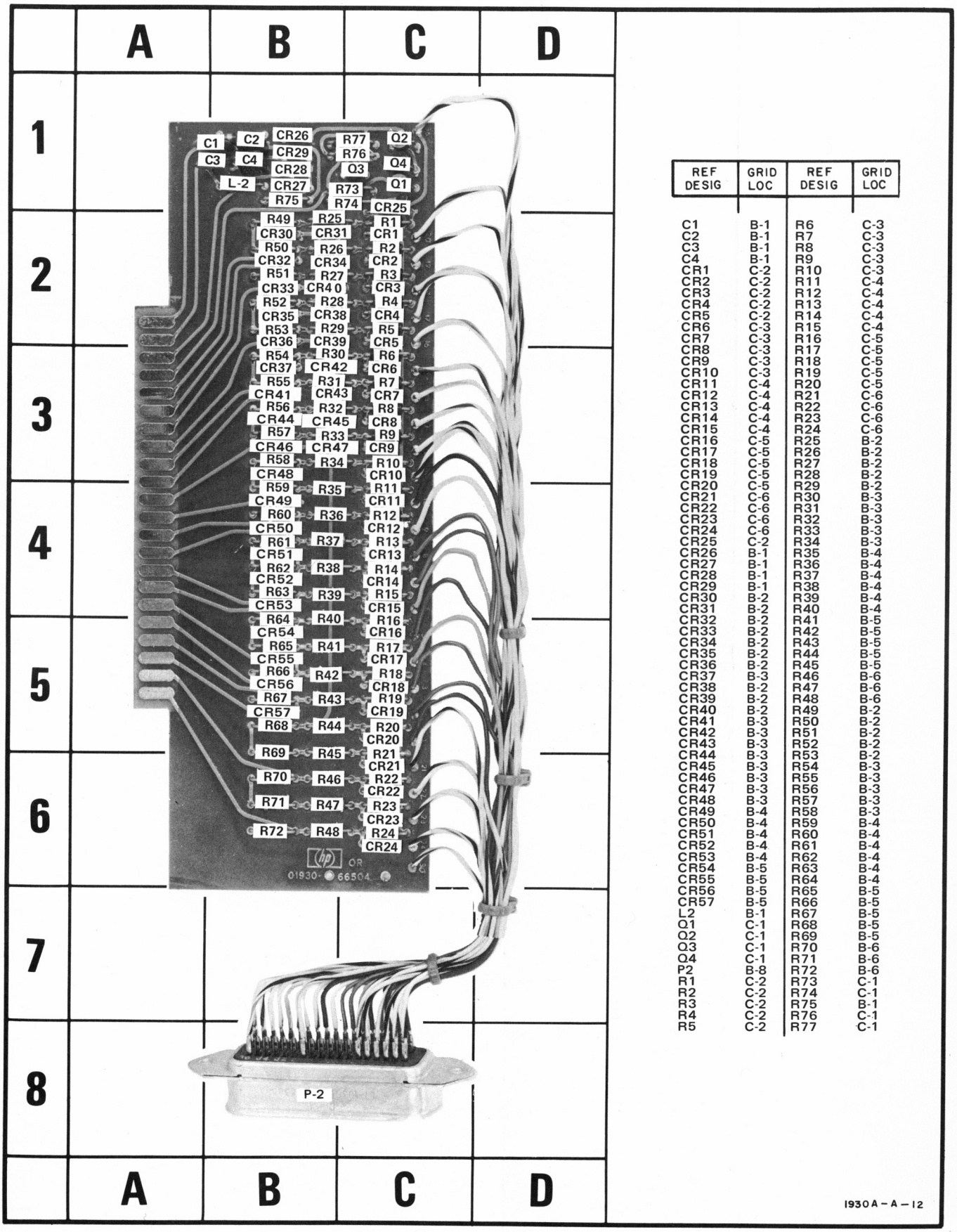
A5
J1

DELETED:

1930A-OUTPUT BUFFERS — 987
1930A — D — 4

5

Figure 8-15.
Output Buffers Schematic



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-1	R6	C-3
C2	B-1	R7	C-3
C3	B-1	R8	C-3
C4	B-1	R9	C-3
CR1	C-2	R10	C-3
CR2	C-2	R11	C-4
CR3	C-2	R12	C-4
CR4	C-2	R13	C-4
CR5	C-2	R14	C-4
CR6	C-3	R15	C-4
CR7	C-3	R16	C-5
CR8	C-3	R17	C-5
CR9	C-3	R18	C-5
CR10	C-3	R19	C-5
CR11	C-4	R20	C-5
CR12	C-4	R21	C-6
CR13	C-4	R22	C-6
CR14	C-4	R23	C-6
CR15	C-4	R24	C-6
CR16	C-5	R25	B-2
CR17	C-5	R26	B-2
CR18	C-5	R27	B-2
CR19	C-5	R28	B-2
CR20	C-5	R29	B-2
CR21	C-6	R30	B-3
CR22	C-6	R31	B-3
CR23	C-6	R32	B-3
CR24	C-6	R33	B-3
CR25	C-2	R34	B-3
CR26	B-1	R35	B-4
CR27	B-1	R36	B-4
CR28	B-1	R37	B-4
CR29	B-1	R38	B-4
CR30	B-2	R39	B-4
CR31	B-2	R40	B-4
CR32	B-2	R41	B-5
CR33	B-2	R42	B-5
CR34	B-2	R43	B-5
CR35	B-2	R44	B-5
CR36	B-2	R45	B-5
CR37	B-3	R46	B-6
CR38	B-2	R47	B-6
CR39	B-2	R48	B-6
CR40	B-2	R49	B-2
CR41	B-3	R50	B-2
CR42	B-3	R51	B-2
CR43	B-3	R52	B-2
CR44	B-3	R53	B-2
CR45	B-3	R54	B-3
CR46	B-3	R55	B-3
CR47	B-3	R56	B-3
CR48	B-3	R57	B-3
CR49	B-4	R58	B-3
CR50	B-4	R59	B-4
CR51	B-4	R60	B-4
CR52	B-4	R61	B-4
CR53	B-4	R62	B-4
CR54	B-5	R63	B-4
CR55	B-5	R64	B-4
CR56	B-5	R65	B-5
CR57	B-5	R66	B-5
L2	B-1	R67	B-5
Q1	C-1	R68	B-5
Q2	C-1	R69	B-5
Q3	C-1	R70	B-6
Q4	C-1	R71	B-6
P2	B-8	R72	B-6
R1	C-2	R73	C-1
R2	C-2	R74	C-1
R3	C-2	R75	B-1
R4	C-2	R76	C-1
R5	C-2	R77	C-1

Figure 8-16. Board Assembly A4 Component Identification

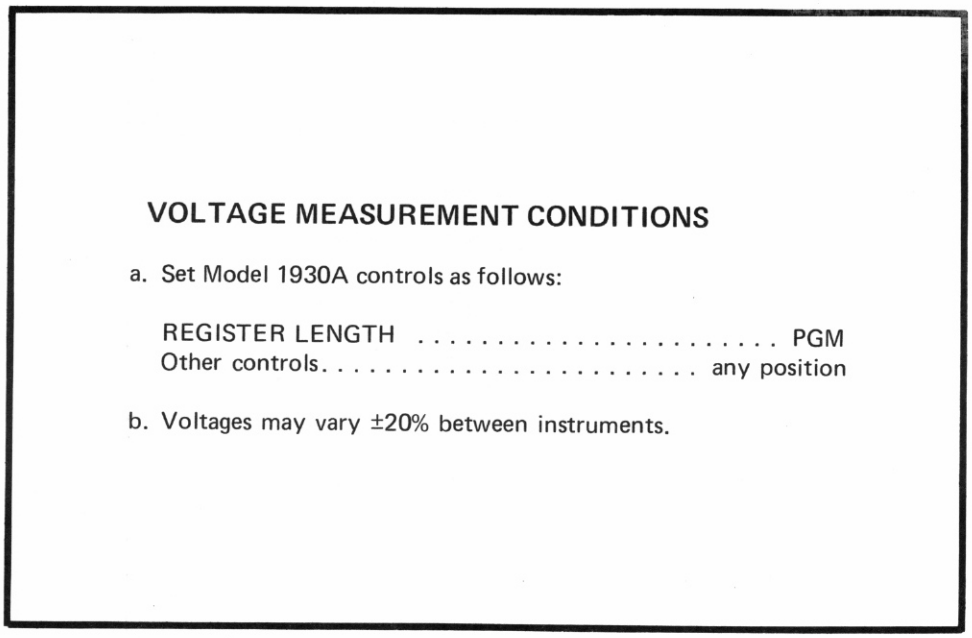


Figure 8-17. Voltage and Waveform Conditions for Schematic 6

PROGRAM INPUT
FROM A4P2

K20 K19 K18 K17 K16 K15 K14 K13 K12 K11 K10 K9 K8 K7 K6 K5 K4 K3 K2 K1 DIV MULT NRZ RESET

(901) (90) (98) (97) (96) (95) (94) (93) (92) (91) (0) (9) (8) (7) (6) (5) (4) (3) (2) (1) (902) (903) (904) (905)

A4
PROGRAM
BOARD

R1 18K CR1 R25 4700 R49 3300
R2 18K CR2 R26 4700 R50 3300
R3 18K CR3 R27 4700 R51 3300
R4 18K CR4 R28 4700 R52 3300
R5 18K CR5 R29 4700 R53 3300
R6 18K CR6 R30 4700 R54 3300
R7 18K CR7 R31 4700 R55 3300
R8 18K CR8 R32 4700 R56 3300
R9 18K CR9 R33 4700 R57 3300
R10 18K CR10 R34 4700 R58 3300
R11 18K CR11 R35 4700 R59 3300
R12 18K CR12 R36 4700 R60 3300
R13 18K CR13 R37 4700 R61 3300
R14 18K CR14 R38 4700 R62 3300
R15 18K CR15 R39 4700 R63 3300
R16 18K CR16 R40 4700 R64 3300
R17 18K CR17 R41 4700 R65 3300
R18 18K CR18 R42 4700 R66 3300
R19 18K CR19 R43 4700 R67 3300
R20 18K CR20 R44 4700 R68 3300
R21 18K CR21 R45 4700 R69 3300
R22 18K CR22 R46 4700 R70 3300
R23 18K CR23 R47 4700 R71 3300
R24 3900 CR24 R48 1000 R72 680

TO PI PIN D
TO PI PIN 6
TO PI PIN 7
TO PI PIN F
TO PI PIN 8
TO PI PIN 9
TO PI PIN K
TO PI PIN 11
TO PI PIN M
TO PI PIN N
TO PI PIN 12
TO PI PIN R → TO P4 PIN 14
TO PI PIN S
TO PI PIN T
TO PI PIN16 → TO PI PIN V
TO PI PIN17
TO PI PIN19
TO PI PIN20 → TO PI PIN X DIV
TO PI PIN 21 MULT
TO PI PIN Y NRZ
TO PI PIN 22 RESET

CR30 CR31 CR32 CR33 CR34 CR35 CR36 CR37 CR38 CR39 CR40 CR41 CR42 CR43 CR44 CR45 CR46 CR47 CR48 CR49 CR50 CR51 CR52 CR53 CR54 CR55 CR56 CR57

FRONT PANEL INPUTS

A5J4 PI

PRBS 20 → E
PRBS 19 → 5
PRBS 17 → H
PRBS 15 → 10
PRBS 13 → L
PRBS 16 → J
PRBS 11 → 13
PRBS 10 → P
PRBS 7 → 15
PRBS 5 → U
PRBS 3 → 18

1

+25 V → 1 → L1 12 → +25VF
C1 .01UF C2 1UF

1 −5.2V → A → L2 12 → −5.2VF
C3 .01UF C4 1UF

B

DIODE LOGIC

MECL OUTPUTS

PROGRAM INPUT
FROM A4P2

K18 K17 K16 K15 K14 K13 K12 K11 K10 K9 K8 K7 K6 K5 K4 K3 K2 K1 DIV MULT NRZ RESET GND

(90) (98) (97) (96) (95) (94) (93) (92) (91) (0) (9) (8) (7) (6) (5) (4) (3) (2) (1) (902) (903) (904) (905)

R3 18K R4 18K R5 18K R6 18K R7 18K R8 18K R9 18K R10 18K R11 18K R12 18K R13 18K R14 18K R15 18K R16 18K R17 18K R18 18K R19 18K R20 18K R21 18K R22 18K R23 18K R24 3900

CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25

R27 4700 R28 4700 R29 4700 R30 4700 R31 4700 R32 4700 R33 4700 R34 4700 R35 4700 R36 4700 R37 4700 R38 4700 R39 4700 R40 4700 R41 4700 R42 4700 R43 4700 R44 4700 R45 4700 R46 4700 R47 4700 R48 1000

R51 3300 R52 3300 R53 3300 R54 3300 R55 3300 R56 3300 R57 3300 R58 3300 R59 3300 R60 3300 R61 3300 R62 3300 R63 3300 R64 3300 R65 3300 R66 3300 R67 3300 R68 3300 R69 3300 R70 3300 R71 3300 R72 680

+25V Q1 +25VF R74 330 R75 5600 R73 5600

Q2 -4.8V CR26 R77 22K -5.2V Q4 +25V -5.2VF

-4.1V Q3 R76 560 -5.2VF

TO PI PIN 6 TO PI PIN 7 TO PI PIN F TO PI PIN 8 TO PI PIN 9 TO PI PIN K TO PI PIN 11 TO PI PIN M TO PI PIN N TO PI PIN 12 TO P4 PIN 14 TO PI PIN R TO PI PIN S TO PI PIN T TO PI PIN16 TO PI PIN V TO PI PIN17 TO PI PIN19 TO PI PIN20 TO PI PIN X DIV TO PI PIN 21 MULT TO PI PIN Y NRZ TO PI PIN 22 RESET

CR32 CR33 CR35 CR34 CR36 CR38 CR39 CR37 CR40 CR41 CR42 CR45 CR44 CR46 CR43 CR47 CR48 CR49 CR50 CR51 CR52 CR53 CR54 CR55 CR56 CR57

DIODE LOGIC

FRONT PANEL ENABLE 1 5

PGM ENABLE | MULT DIV ENABLE | NRZ ENABLE | RESET ENABLE | SYNC DTL

A5J4 P1 4 C 3 2 Z

CR27 CR29 CR28 +25V

(906) SYNC DTL A4P2 PIN30

PI A5J4

FROM CR30	D	K20
FROM CR32	6	K19
FROM CR33	7	K18
FROM CR35	F	K17
FROM CR36	8	K16
FROM CR37	9	K15
FROM CR38	K	K14
FROM CR42	11	K13
FROM CR46	M	K12
FROM CR48	N	K11
FROM R49	12	K10
FROM CR50	R	K9
FROM R61	14	K8
FROM CR51	S	K7
FROM CR53	T	K6
FROM CR54	16	K5
FROM R65	V	K4
FROM CR55	17	K3
FROM CR57	19	K2
FROM CR45	20	K1
FROM R69	X	$\overline{DIV}$
FROM R70	21	$\overline{MULT}$
FROM R71	Y	NRZ
FROM R72	22	RESET

3 4 1

MECL OUTPUTS

1930A-PROGRAMER-987 1930A-E-2

REFERENCE DESIGNATIONS

A4
C1-C4 CR1-CR57 L1-L2 Q1-Q4 R1-R77
A5
J4

DELETED:

6

Figure 8-18.
Programming Board Schematic

MANUAL CHANGES

MODEL 1930A

PSEUDO RANDOM BINARY SEQUENCE GENERATOR

Manual Serial Prefixed: 0987A
Manual Print Date: FEB 1971

Make all changes listed below as Errata. Check the following table for your instrument serial prefix and/or serial number and make listed change(s) to the manual:

Serial Prefix or Number	Make Changes
1109A	1
1119A	1 and 2
1126A	2 and 3
1212A	2 thru 4

Serial Prefix or Number	Make Changes

ERRATA

Page 1-1, Paragraph 1-14,
Change 5060-0459 to read: 5060-0460.

Page 4-4, Figure 4-4,
Change the all zero detector from a NOR gate to an OR gate.
In the table, delete the negating bars from the "Q"s.
Change the F/F outputs in line 2 to read 110.
Change the F/F outputs in line 3 to read 011.

Page 4-9, Paragraph 4-84,
Change third line to read: NOR gate A1U2A, OR/NOR gate A1U1A and OR.

Page 4-9, Paragraph 4-96,
Change first and second lines to read: 4-96. The multiply gate, consisting of A2U22B, A2U22C, A2U12B and A2U12C, determines the input function of A2U10.

Page 4-11, Paragraph 4-128,
In the second line, delete "A1R37 and".

Page 4-11, Paragraph 4-130,,
Change 3×10^{-2} (line 3) to 2×10^{-2}.

Page 5-0, Table 5-1,
Change electronic counter from HP 5345L/M to 5245L/M.

Page 5-4, Paragraph 5-17f,
In the last line, change Table 3-3 to read Table 3-1.

Δ Table 6-2,
A4Q4: Change to HP Part No. 1854-0215, TSTR:SI NPN, Mfr. Code 80131, Mfr. Part No. 2N3904.

Page 8-7, Figure 8-1,
Change: in block directly above block 3, collector of A1Q7 to read: base of A1Q7.
Change block 6 as follows:
delete line reading Pin 7 CL pulses.
change line reading Pin 8 Logic "1" to Pin 9 Logic "1".

Page 8-11, Figure 8-7,
Change designator of R58 (located in base circuit of Q6) to R59.

Page 8-13, Figure 8-10,
U9B: Change pin 3 to read 4.
U17B: Change pin 3 to read 6.
U18A: Change pin 6 (input) to read 5.
U18B: Delete negating bar. Change pin 4 to read 3.
U18C: Change pin 9 to read 13. Change pin 10 to read 12. Change pin 8 to read 11.

Page 8-15, Figure 8-13,
Delete the negating bar from the mathematical term at the output of U15C and add it to the mathematical term at the output of U15D.

Page 8-17, Figure 8-15,
C14: Relocate between junction of R26/U3A-11 and ground.
Change A5J1 pin L to pin K.
Change A5J1 pin K to pin J.

Δ Page 8-18, Figure 8-16,
Q3: Change reference designator to Q2.
Q2: Change reference designator to Q3.

Δ Page 8-19, Figure 8-18,
A4Q4: Show symbol as NPN transistor.

Page 8-20, Figure 8-19,
Change the caption on the line between A1 pin 8 and A2 pin U from IM to ID.

17 September 1973
Δ = Latest additions to this change sheet.
This change sheet supersedes all prior change sheets for this manual.

Supplement A for
01930-90901

CHANGE 1

Page 3-2, Paragraph 3-43,
Add: "In NORM" at beginning of paragraph.
Page 4-1, Paragraph 4-16,
Add: "In NORM" at beginning of paragraph.
Page 4-3, between paragraph 4-39 and 4-40,
Add:

Note

To operate in this mode, the wire between S4 (Figure 8-4) and A5J3-pin 3 must be disconnected.

Page 4-10, between Paragraphs 4-100 and 4-101,
Add:

Note

The zero detector operates only in NORM.

Table 6-2,
Add: A5CR1, 1901-0040 DIODE: SILICON 30 MA 30 WV, Mfr. Code 07263, Mfr. Part No. FDG 1088.

Table 6-2 (Cont'd),
S4: Change to HP Part No. 3101-0939, SWITCH: TOGGLE DPDT 5A 115 VAC, Mfr. Code 09353; Mfr. Part No. 7203.
Page 8-5/8-6, between paragraph 8-41 and 8-42,
Add:

Note

To operate as described in paragraph 8-41 above, the wire between S4 and A5J3-3 must be disconnected.

Page 8-5/8-6, Paragraph 8-45,
Add:
a. Disconnect wire between S4 and A5J3, pin 3.
Change: subpara a to b.
subpara b to c.
subpara c to d.
subpara d to e.
Add: f. When troubleshooting is completed, reconnect wire between S4 and A5J3, pin 3.
Page 8-9, Figure 8-4,
Change schematic as shown in Figure 1.

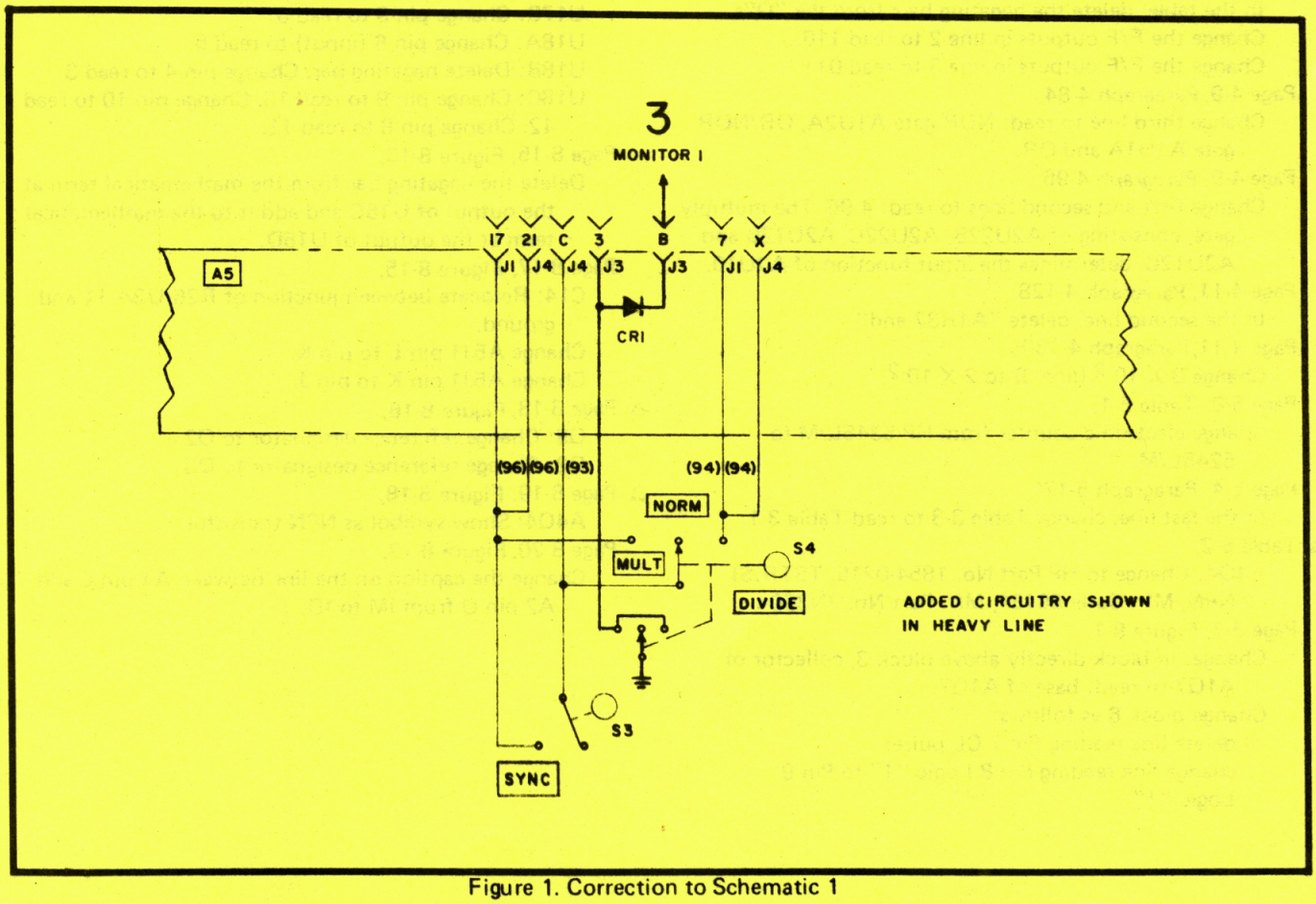


Figure 1. Correction to Schematic 1

CHANGE 2

Page 5-6,
Change Paragraph 5-22 to read as follows:
5-22. The Model 1930A adjustments are located under screwdriver access holes in the top cover. BIAS ADJUST A1R9 is located near the rear of the instrument. SYMMETRY ADJUST A1R58 is located about the middle of the instrument.
Section V,
Add: page 5-6c (attached to this change).
Table 6-2,
A1: Change HP Part No. and Mfr. Part No. to 01930-66508.

Table 6-2 (Cont'd),
A1C1, A1C5, A1C8, A1C12, A1C15-A1C17, A1C20-A1C23: Change HP Part No. and Mfr. Part No. to 0160-3451.
A1C4: Change HP Part No. to 0160-3443; C: FXD TA 1 UF 35 VDCW, Mfr. Code 72982; Mfr. Part No. 8131-050-651-104Z.
Add: A1R58, HP Part No. 2100-2413, R: VAR FLM 200 OHM 10% LIN 1/2W, Mfr. Code 28480; Mfr. Part No. 2100-2413.
Page 8-17, Figure 8-15,
C14: Change value to 0.1 UF.
Add: R58, 200 ohms, between R44 and junction of of R38 and R43.
Connect rotor to junction. Label control SYMMETRY ADJUST.

CHANGE 3

Page 3-2, Paragraph 3-43,
Add: "In NORM" at beginning of paragraph.
Page 4-1, Paragraph 4-6,
Add: "In NORM" at beginning of paragraph.
Page 4-3, following Paragraph 4-39,
Add:

Note

To operate in this mode, the all zero inhibitor circuit must be disabled. This can be done by temporarily grounding the base of A3Q4.

Page 4-10, following Paragraph 4-100,
Add:

Note

The zero detector operates only in NORM.

Add:

4-105A. ALL ZERO INHIBITOR CIRCUIT. (See Schematic 4.)

4-105B. The all zero inhibitor circuit consists of A3U18D, A3Q3 and A3Q4. In cryptography, the all-zero condition is a legitimate condition and the all zero detector, by acting to prevent this condition, introduces an error. To correct this, the all zero inhibitor circuit disables the all zero detector in MULTIPLY and DIVIDE (encode and decode).

4-105C. In NORM, pins 9 and 10 of NOR gate A3U18D are at logic 0 and pin 8 is a logic 1, causing Q3 and Q4 to be turned off. CR1 is back biased and the MONITOR 1 line follows the Q outputs of A3U8, U5, U3, U15, and U16. In MULTIPLY or DIVIDE, either pin 9 or pin 10 of A3U18D goes to logic 1 and pin 8 goes to logic 0. A3Q3 and A3Q4 turn on. A3CR1 is forward biased and the MONITOR 1 line is clamped at logic 1.

ΔPage 5-4, following paragraph 5-16 step o,
Add:

Note

To perform the following checks, the all zero detector must be disabled. This can be done by temporarily grounding the base of A3Q4.

Table 6-2,
Add: A3CR1; HP Part No. 1901-0040, DIODE: SILICON 30 MA 30 WV, Mfr. Code 07263, Mfr. Part No. FDG 1088.
Add: A3Q3, A3Q4; HP Part No. 1853-0086, TSTR: SI PNP, Mfr. Code 80131, Mfr. Part No. 2N5087.
Add: A3R16, A3R18; HP Part No. 0684-5621, R: FXD COMP 5.6K OHM 10% 1/4W, Mfr. Code 01121, Mfr. Part No. CB 5621.
Add: A3R17: HP Part No. 0684-2711, R: FXD COMP 270 OHM 10% 1/4W, Mfr. Code 01121; Mfr. Part No.CB 2711.
A3: Change HP Part No. and Mfr. Part No. to 01930-66506.
A3R1: Change to HP Part No. 0684-4711, R: FXD COMP 470 OHM 10% 1/4W, Mfr. Code 01121; Mfr. Part No. CB 4711.
A3R6, A3R10, A3R14: Change to HP Part No. 0698-7025, R: FXD COMP 270 OHM 10% 1/8W, Mfr. Code 01121; Mfr. Part No. BB 2711.
A3R7, A3R9, A3R11, A3R13, A3R15: Change to HP Part No. 0698-7936, R: FXD COMP 160 OHM 5% 1/8W, Mfr. Code 01121; Mfr. Part No. BB 1615.
A6: Change to HP Part No. and Mfr. Part No. 01930-60001.
Page 8-5/8-6, following Paragraph 8-41,
Add:

Note

To operate in this mode, the all zero inhibitor circuit must be disabled. This can be done by temporarily grounding the base of A3Q4.

CHANGE 3 (Cont'd)

Page 8-5/8-6, Paragraph 8-45,
Add:
a. Jumper base of A3Q4 to ground.
Change: subpara a to b.
subpara b to c.
subpara c to d.
subpara d to e.

Page 8-5/8-6, Paragraph 8-45 (Cont'd),
Add:
f. When troubleshooting is completed, disconnect jumper from base of A3Q4.

Page 8-11, Figure 8-7,
Change schematic as shown in Figure 2.

ΔPage 8-12,
Replace figure 8-8 with attached figure 8-8.

Page 8-13, Figure 8-10,
Change schematic as shown in Figure 3.

CHANGE 4

Table 6-2,
MP4: Change to HP Part No. 01930-60201, PANEL: MINT-GRAY, Mfr. Code 28480; Mfr. Part No. 01930-60201.
MP5: Change to HP Part No. 01930-20202, FRAME: PANEL MINT-GRAY Mfr. Code 28480; Mfr. Part No. 01930-20202.

Table 6-2 (Cont'd),
MP7: Change to HP Part No. 0370-2136, KNOB: JADE-GRAY, Mfr. Code 28480; Mfr. Part No. 0370-2136.

5-25. SYMMETRY ADJUST.

a. Connect equipment as shown in Figure 5-9.

b. Adjust clock generator for output between 10 and 25 MHz.

c. Adjust oscilloscope to view 2-volt 10-ns pulse.

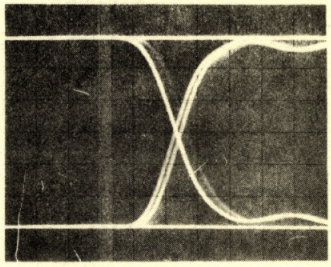
d. Set Model 1930A controls as follows:

REGISTER LENGTH 20
PRBS/WORK . . . . . PRBS
MULTIPLY/NORM/DIVIDE . . . . . NORM
NRZ/RZ . . . . . NRZ

e. Oscilloscope will alternately display leading edge and trailing edge to form symmetrical X. (See Figure 5-10.) Adjust A1R58 to bring crossover point of X to middle (50% amplitude point) of display.

f. Check jitter at crossover point. Jitter must be less than 2 ns peak-to-peak.

g. Disconnect PRBS output and connect ERROR output to oscilloscope. Verify that amplitude of error pulse still meets specification.



Sweep Speed ≅ 2 ns/div

Vert. Sens. ≅ 3 v/div

Figure 5-9. Symmetry Adjust Setup

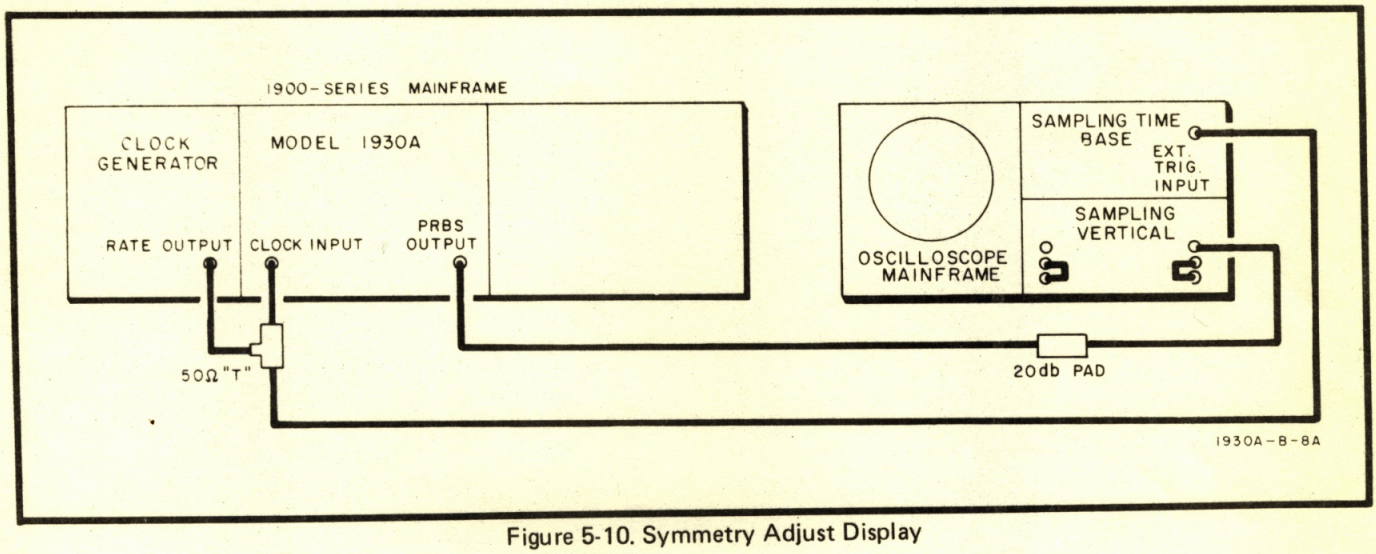
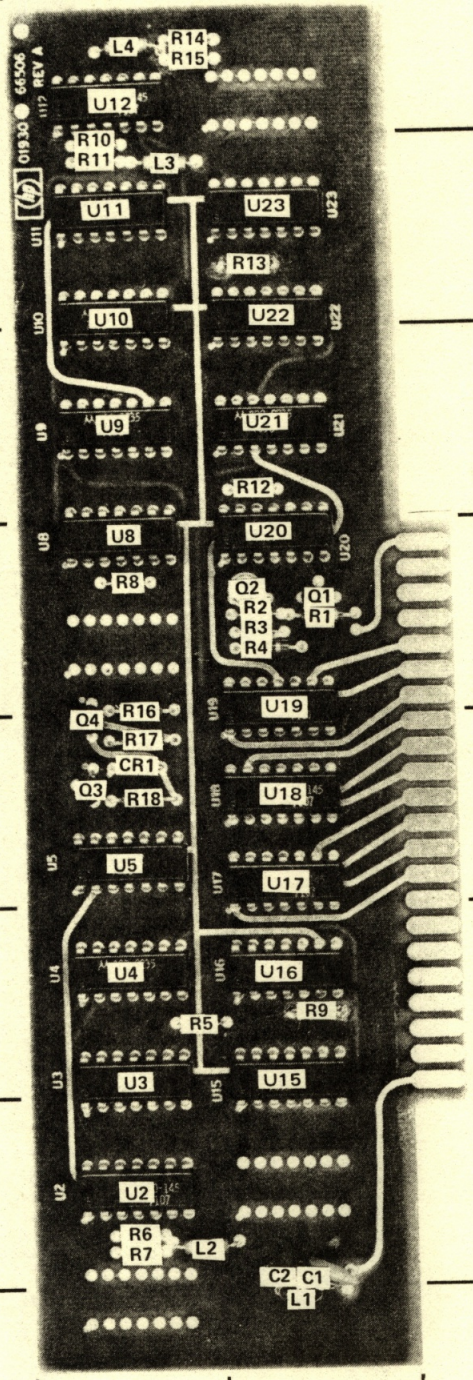


Figure 5-10. Symmetry Adjust Display



REF DESIG	GRID LOC
C1	C-7
C2	C-7
CR1	B-5
L1	C-8
L2	B-7
L3	B-2
L4	B-1
Q1	C-4
Q2	C-4
Q3	B-5
Q4	B-5
R1	C-4
R2	C-4
R3	C-4
R4	C-4
R5	B-6
R6	B-7
R7	B-7
R8	B-4
R9	C-6
R10	B-2
R11	B-2
R12	C-3
R13	C-2
R14	B-1
R15	B-1
R16	B-4
R17	B-5
R18	B-5
U2	B-7
U3	B-6
U4	B-6
U5	B-5
U8	B-4
U9	B-3
U10	B-2
U11	B-2
U12	B-1
U15	C-6
U16	C-6
U17	C-5
U18	C-5
U19	C-4
U20	C-4
U21	C-3
U22	C-2
U23	C-2

1930A-R-1

Figure 8-8. Board Assembly A3 Component Identification

OPTIONS

Page 7-1/7-2,
Add the following paragraph:
7-11. OPTION X95. Optional color. Light gray panel and panel frame with a black knob. Make the following changes to table 6-2.
MP4: Change to HP Part No. 01930-00201, PANEL: FRONT LIGHT GRAY, Mfr. Code 28480; Mfr. Part No. 01930-00201.

Page 7-1/7-2 (Cont'd),
MP5: Change to HP Part No. 01930-20201, FRAME: PANEL LIGHT GRAY, Mfr. Code 28480; Mfr. Part No. 01930-20201.
MP7: Change to HP Part No. 01930-67401, KNOB: BLACK, Mfr. Code 28480; Mfr. Part No. 01930-67401.

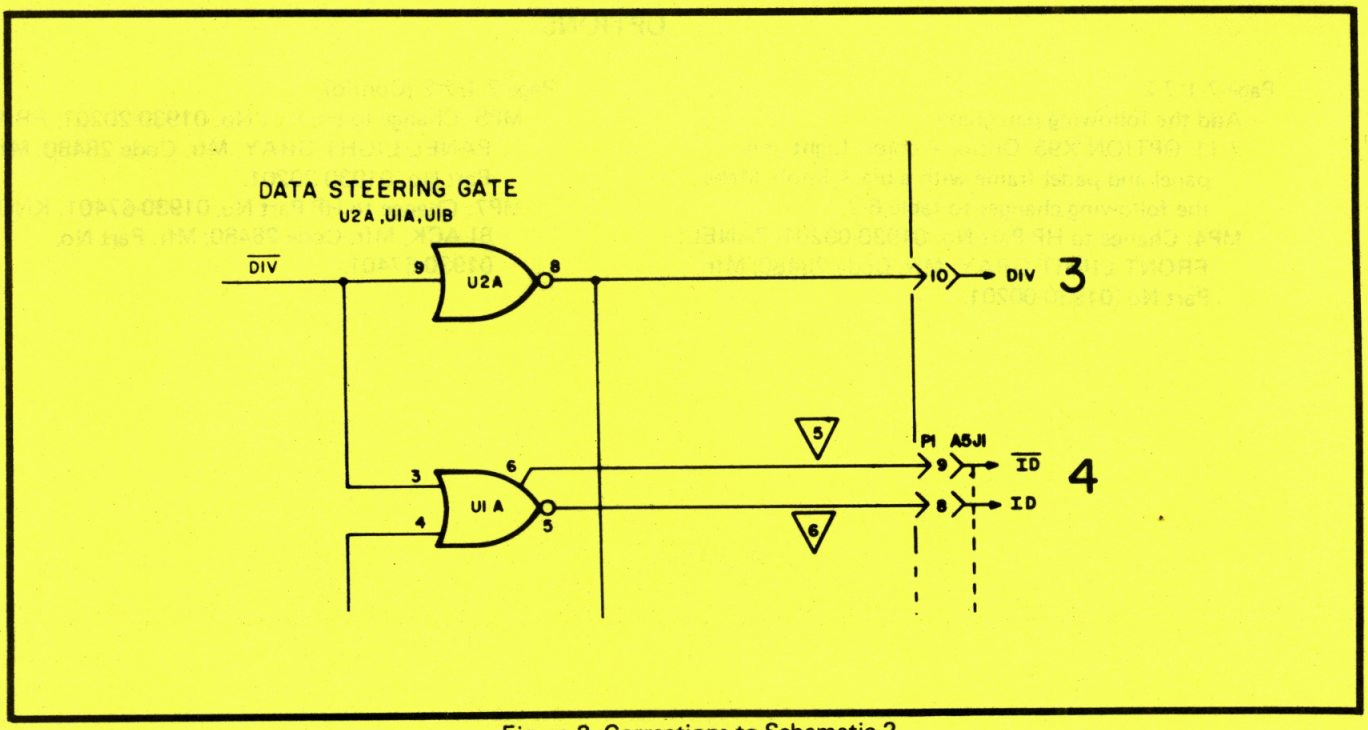


Figure 2. Corrections to Schematic 2

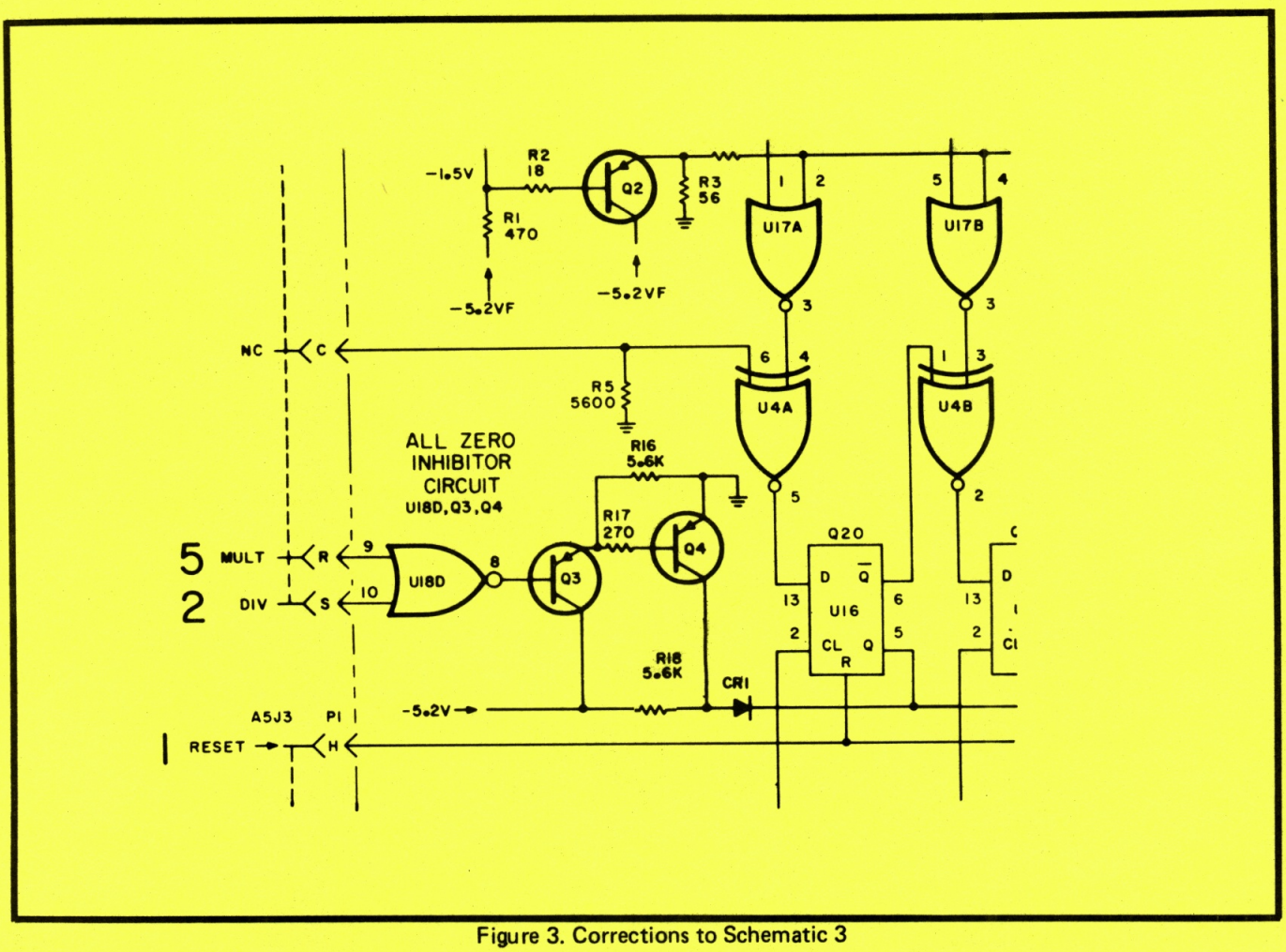


Figure 3. Corrections to Schematic 3