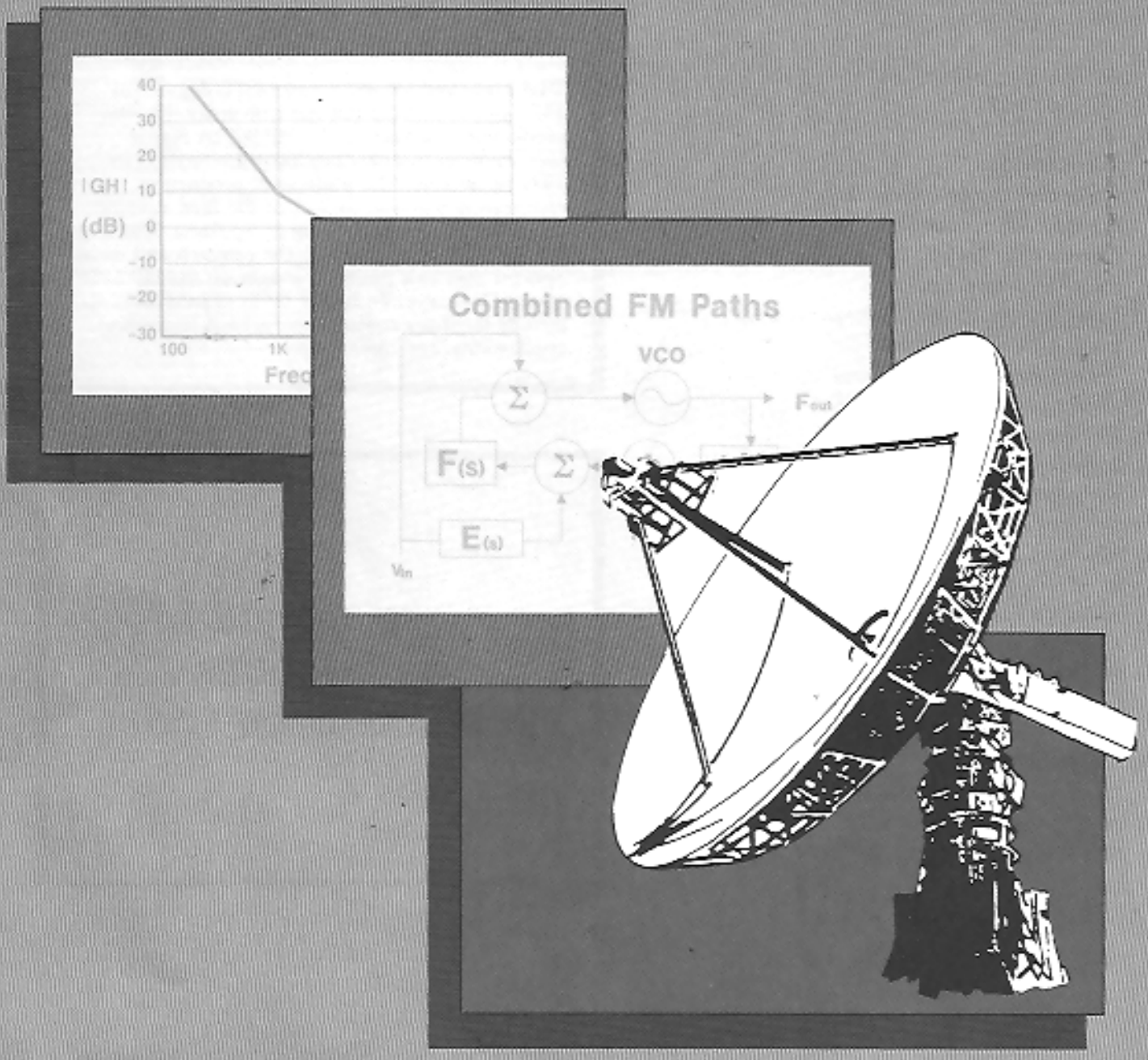
RF & Microwave Measurement Symposium and Exhibition

FM Design Techniques in Phase Lock Loops

David Whipple



FM Design Techniques in Phase Lock Loops

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Biography

David Whipple

David received his BSEE and MSEE degrees in 1972 and 1973 from Purdue University. He was production engineer on the HP 8672A Signal Generator for the new product introduction. In 1979 he accepted the position of production engineering manager as part of the first wave of transfers to the new division in Spokane, Washington. In 1981 he moved into the research and development area as a project manager on the HP 8656B Signal Generator. Technical fields of interest include feedback control theory, high-frequency applications, and metrology.

FM DESIGN TECHNIQUES IN PHASE LOCK LOOPS

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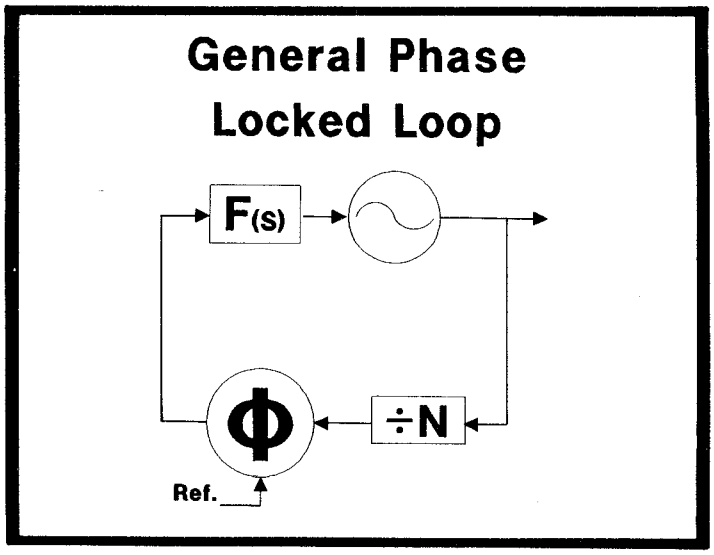
The Phase Locked Loop is the general building block of today's indirect synthesizers. Their use in signal generators is widespread. The mathematical model of the phased locked loop uses linear feedback control theory. Building blocks are a voltage controlled oscillator (VCO), a divide by N block, a phase detector, a block simply labeled F(s) which is the gain, poles, and zeroes needed for lock, and a suitable reference frequency.



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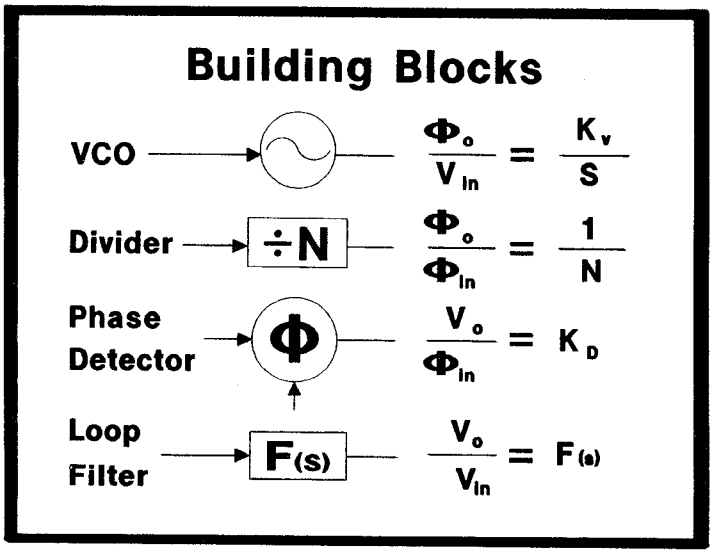
The equations of motion for each of the blocks is shown here. The VCO is characterized as having a linear relationship of frequency vs voltage at any given operating point. We shall see later that the lack of constant sensitivity as a function of frequency can be a major problem. Note that in all the blocks, the variables of interest are voltage and phase (not frequency). The Laplace operator,"s", in the denominator of the VCO equation indicates that its relation between voltage and phase is that of an integrator. This is because phase is the integral of frequency, or conversely, the derivative of phase is frequency.

The divide by N block is a linear operator. By this I mean that the 1/N equation holds for phase as well as frequency.

The phase detector has a constant gain, Kv, which relates output voltage to input phase difference.



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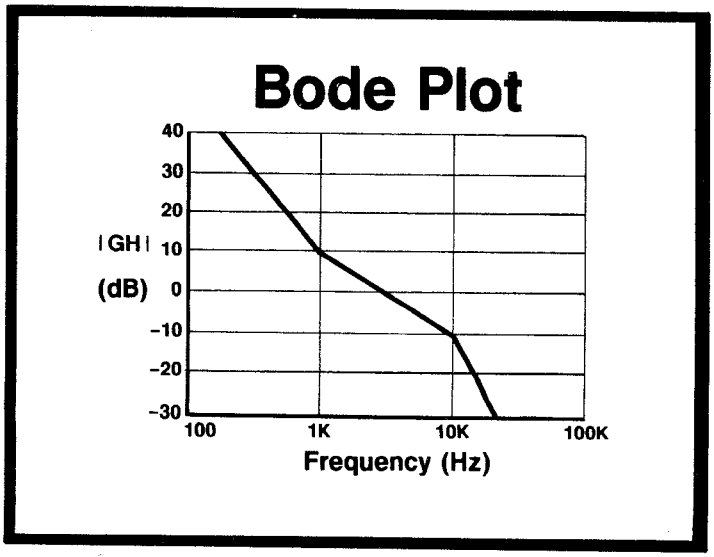
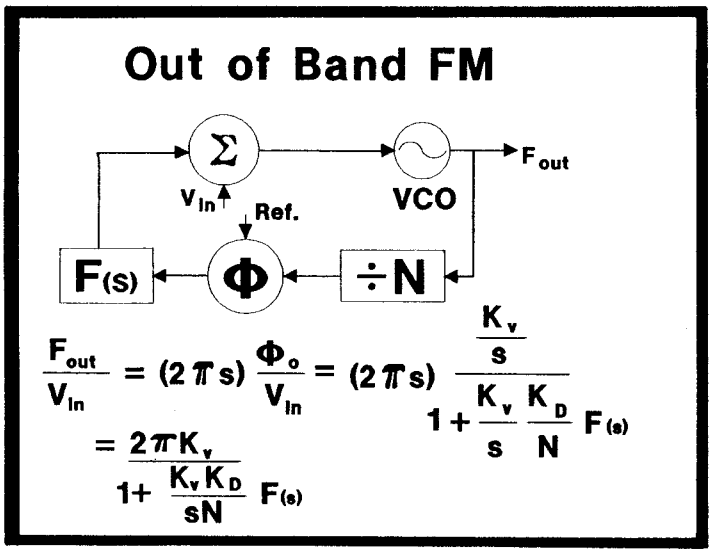
The F(s) block contains gain and filtering and sets the loop bandwidth. It will be assumed that there is a gain term, an integrator, a zero for stability, and another pole which will result in a loop Bode plot that looks something like this:

The loop bandwidth is chosen for reasons of noise, switching speed, spurious rejection, and information bandwidth.





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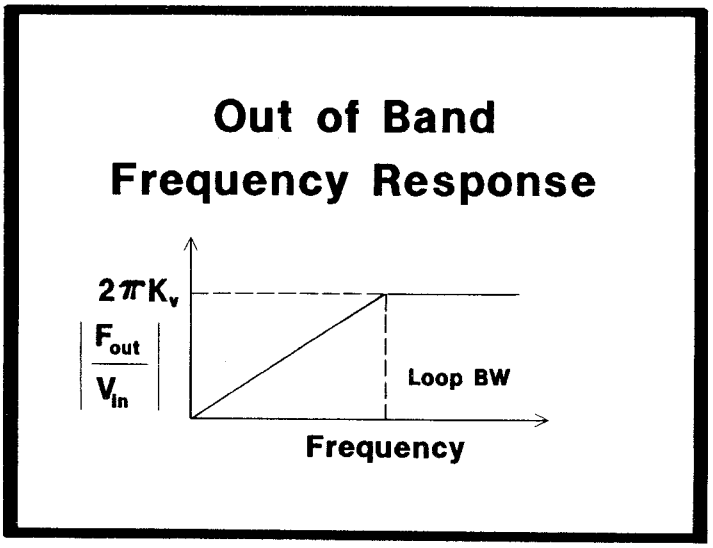
It is often desirable to frequency modulate the oscillator in a PLL. This works moderately well for frequencies beyond the loop bandwidth, but at lower modulating frequencies the loop tries to remove the modulation. This can be seen by looking at the transfer function for this input.



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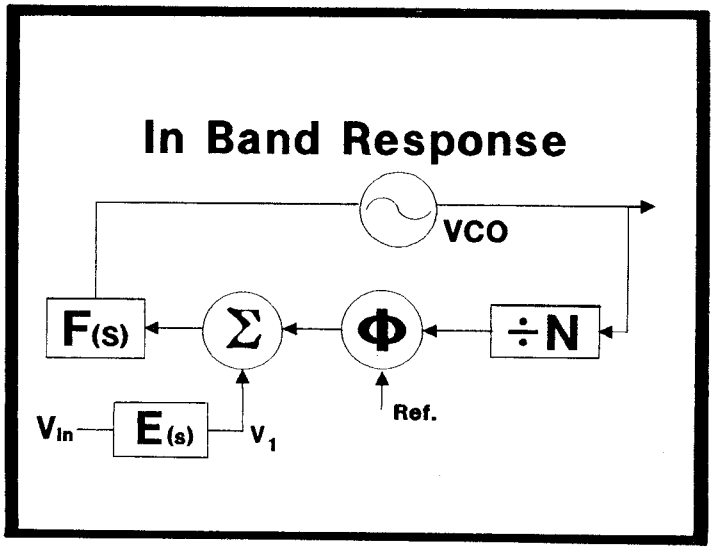
This is the typical frequency response of the transfer function. For this I assumed that F(s) is a low pass response at high frequencies.



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The modulation bandwidth often needs to extend to rates lower than the loop bandwidth. In this case, the modulation is preconditioned by a block which I label E(s) and then summed in at the output of the phase detector. E(s) is an integrator.

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Shown here is the transfer function for this input.

In Band Response

$$\frac{\Phi_o}{V_1} = \frac{F(s)\frac{K_v}{s}}{1 + \frac{K_v}{s}\frac{K_D}{N}F(s)}$$

$$\frac{F_{out}}{V_{in}} = \left(\frac{2\pi s}{1/E(s)}\right)\left(\frac{\Phi_o}{V_1}\right) = \frac{2\pi F(s) K_v E(s)}{\left(1 + \frac{K_v}{s}\frac{K_D}{N}F(s)\right)}$$

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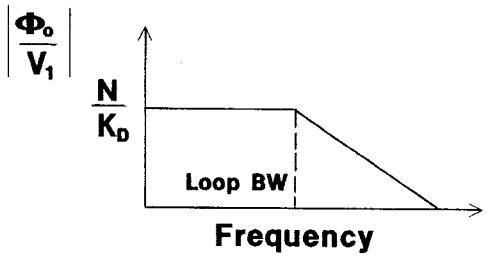
This is the typical frequency response. Note that the vertical scale is phase in this case. If E(s) is an integrator, then FM vs Vin will have the same shape.

In Band Frequency Response



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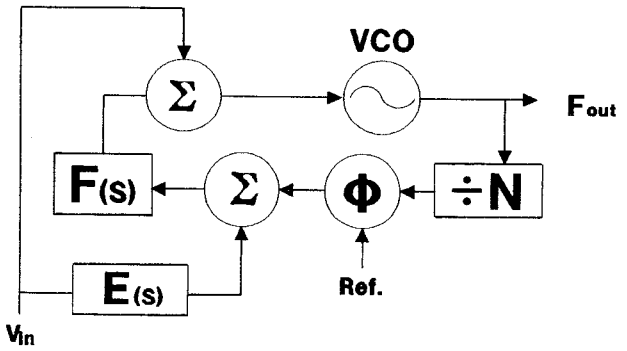
The out-of-band, high-pass response and the in-band, low-pass response are governed by the loop dynamics. When added with appropriate gain, the FM response is flat.

Combined FM Paths



Combined FM Paths

$$\frac{F_{out}}{V_{in}} = \frac{2\pi K_v \, F(s) \, E(s) + 2\pi K_v}{1 + \frac{K_v}{s}\frac{K_D}{N} F(s)}$$

$$= 2\pi K_v \, \frac{1 + E(s) \, F(s)}{1 + \frac{K_v}{s}\frac{K_D}{N} F(s)}$$

For Flat Response, Zeroes = Poles or

$$E(s) = \frac{K_v \, K_D}{Ns}$$

1182

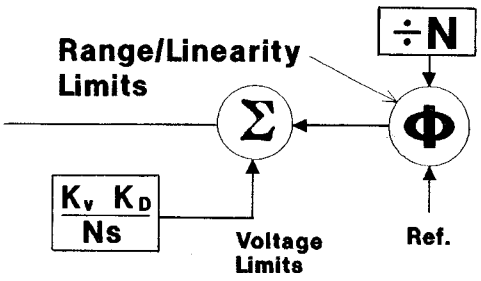
When the two paths are used in parallel, superposition gives the total response. If the frequency response is to be flat, the poles and zeroes must be in the same locations, or

$$E(s) = \frac{KvKd}{N\,s}$$

It should be noted here that the frequency response is flat, but the sensitivity changes with both Kv and N. If the PLL is to have a known sensitivity, then both Kv and N must be taken into account.

Note that E(s) is an integrator. If the Kv of the oscillator and the Divide number N of the loop are constant, then the FM sensitivity is held constant. These constraints mean that the PLL must operate at a constant center frequency, or that additional compensation circuits be added.

Phase Deviation Limits



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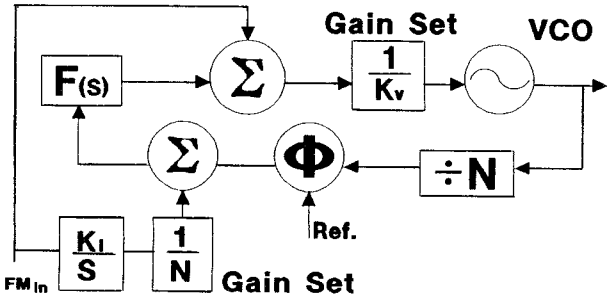
One of the physical limitations is the maximum phase deviation, or modulation index, Beta (FM deviation divided by FM rate). This is usually set by the dynamic range of either the phase detector or the FM integrator. The larger the divide number, N, the larger the Beta can be because the angular displacement seen by the phase detector multiplies by N at the VCO. The output of the FM integrator also multiplies by N to the VCO.

The negative aspect of the large divide number is that the loop bandwidth is very narrow. This causes the loop to be more susceptible to microphonics and the residual FM might not be as good as could be with a wider bandwidth.

Gain Correction in Variable Frequency Loop



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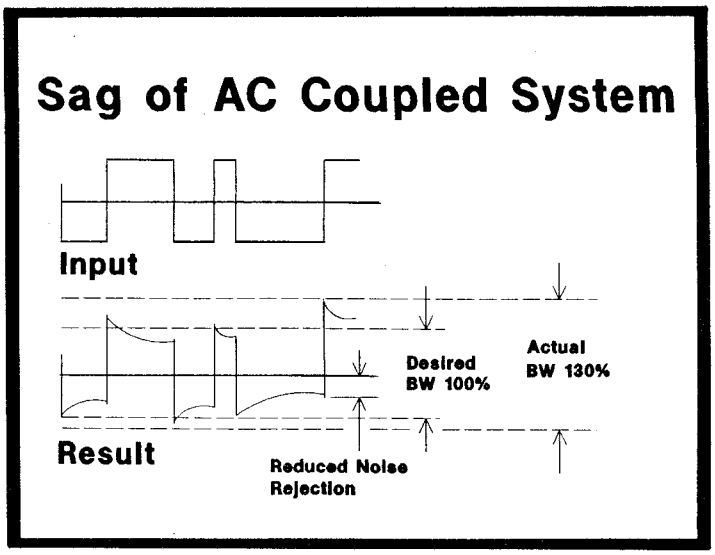
A major decision to be made in the initial design of a signal generator is how to implement FM. The decision is whether to increase the complexity in the number of phase locked loops (a dedicated FM loop), or to implement FM in a variable frequency loop (correction for changing Kv and N). In general, higher performance is achieved in a dedicated loop.

1185
A feature that is becoming increasingly important is DC coupled FM. Digital radio manufacturers' use DCFM to improve the accuracy of test signals. AC coupled FM converts square waves into exponentials. This does two things. First, it approaches the digital thresholds as the test stimulus sags. This can significantly degrade the bit error rate, particularly at low signal levels.

The other negative effect is an expansion of the RF signal. Stated another way, the center frequency walks around, possibly straying outside radio's IF bandwidth.



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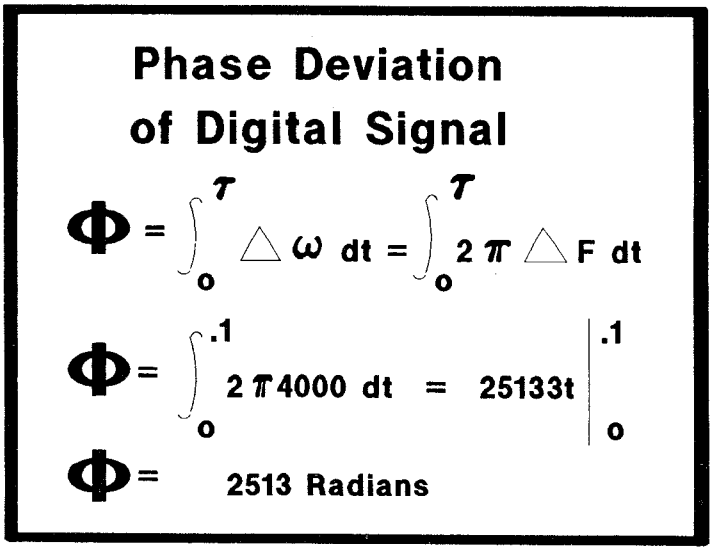
Another limitation of AC coupled FM is the maximum allowable modulation index, beta. The actual limit may be due to either the FM integrator or the phase detector. A long string of 1's or 0's results in an extremely large beta. For instance, a 4 kHz deviation will accumulate more than 2500 radians in only .1 second. This is not an unreasonable demand for a signal generator.



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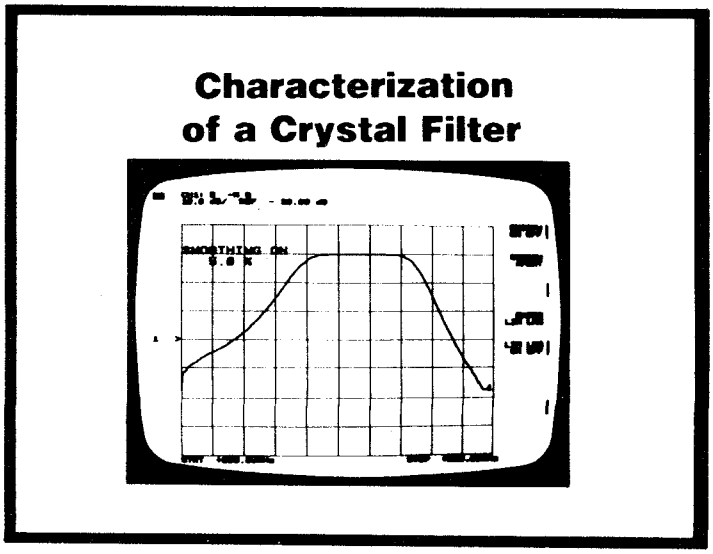
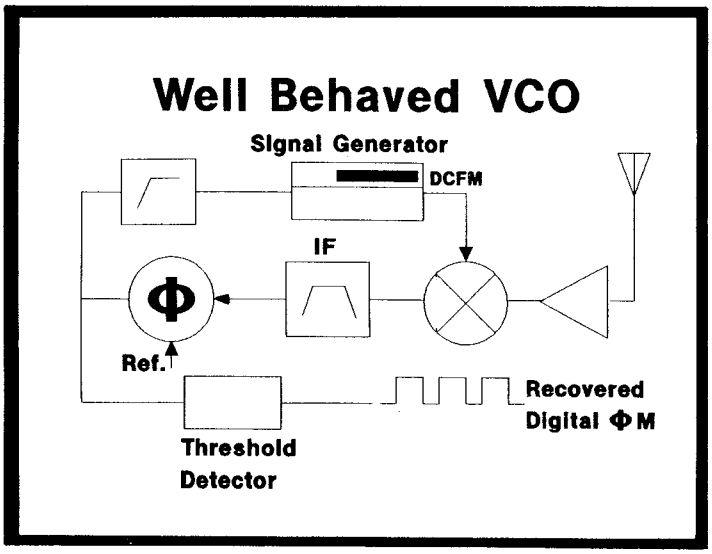
Signal Generators are often used as a general purpose stimulus. The HP 8505A (opt 005) allows for an external source which is needed to test narrow band devices. This basically makes a clean narrow band sweeper out of the signal generator.





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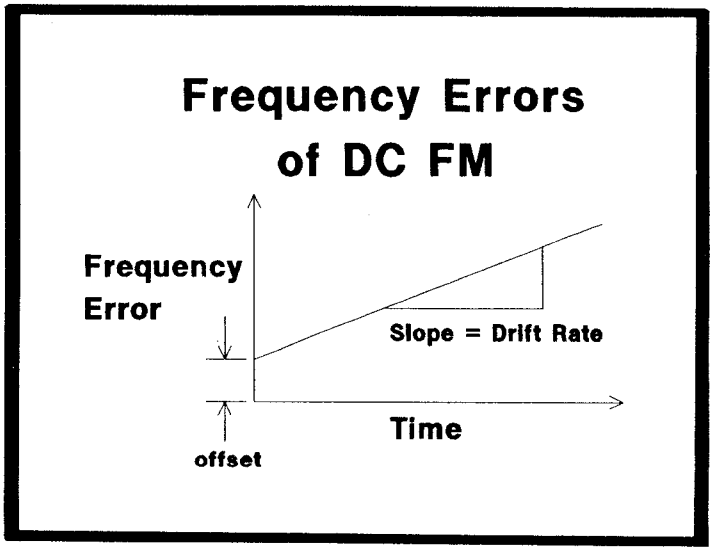
Another application is as a well behaved VCO. In this example, the signal generator is the local oscillator for a phase locked receiver. The DC FM port is the feedback path to enable the receiver to lock.



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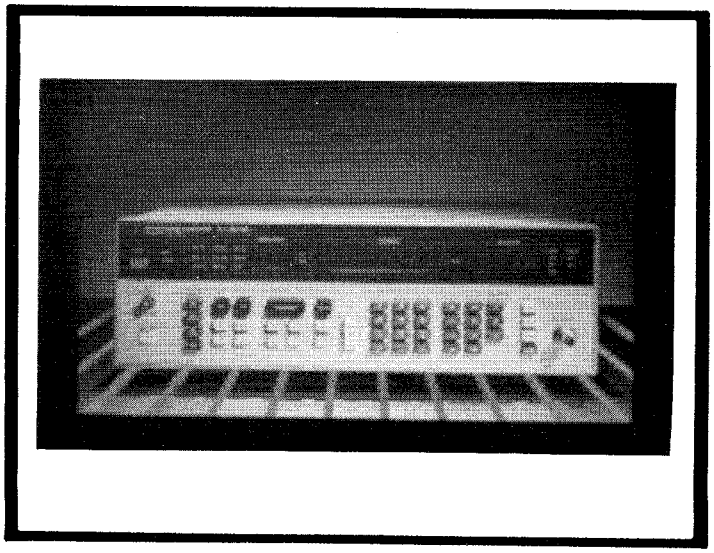
DC FM provides exact signal representation. There is no sag, and it allows for infinite beta. There are, however, tradeoffs. The center frequency is no longer locked to the reference which results in frequency offset and frequency drift. DC FM is usually implemented with an unlocked VCO. Several instruments use internal calibration to reduce the frequency offset. The frequency drift remains. Typical radio requirements are for total frequency error to be less than 500 Hz.



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The HP 8656B sets new standards for DC FM performance. A technology has been developed to dramatically improve DC FM. This method allows center frequency accuracy to be specified at better than 500 Hz over all center frequencies, deviations, and environmental conditions (0–55°C, 95% humidity).

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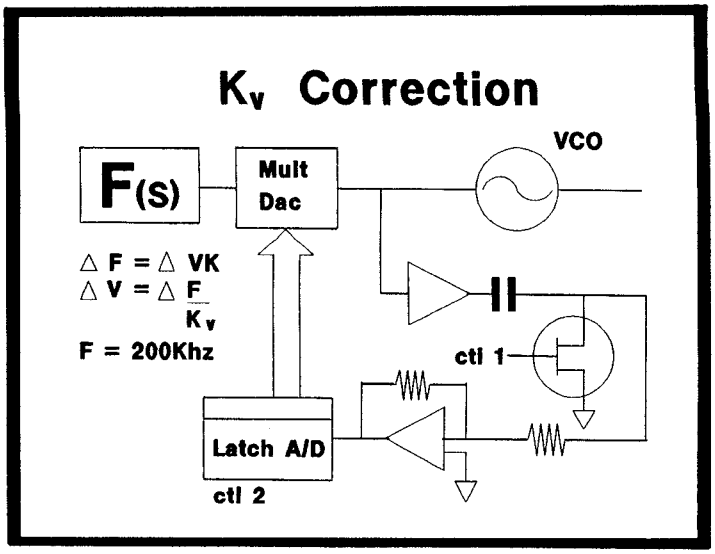
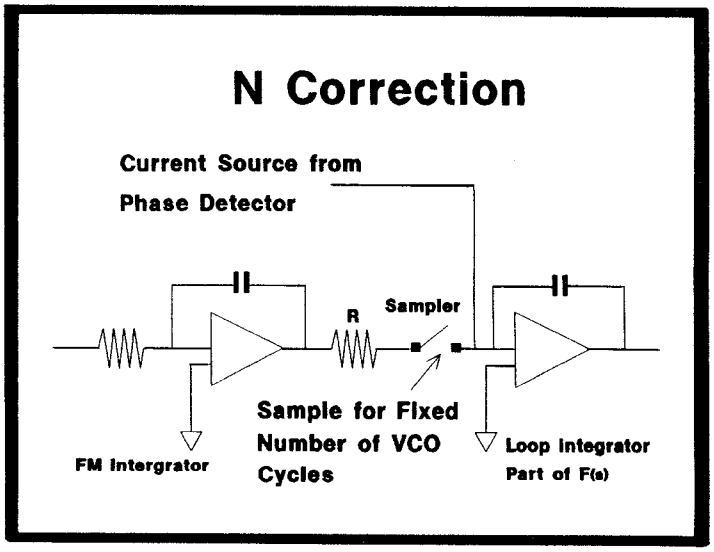
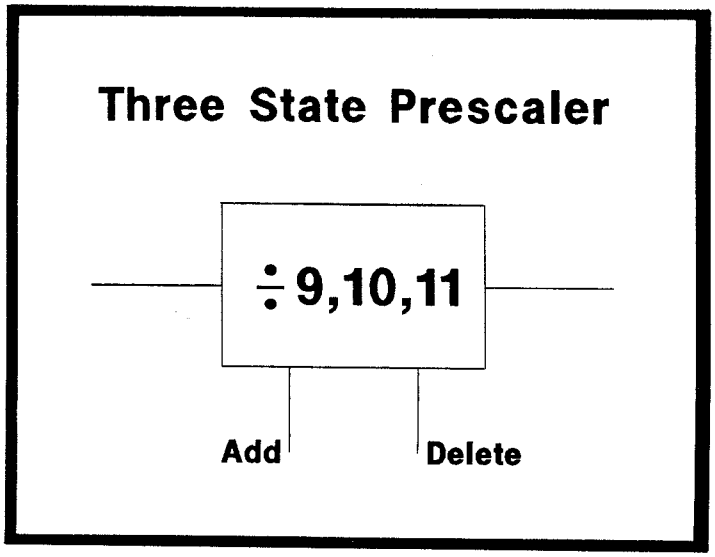
The HP 8656B uses a variable frequency loop for FM generation, as did the HP 8656A. This requires additional circuitry to compensate for changes in the VCO sensitivity, Kv, and for the variable N number of the loop. Shown here is the Kv compensation.

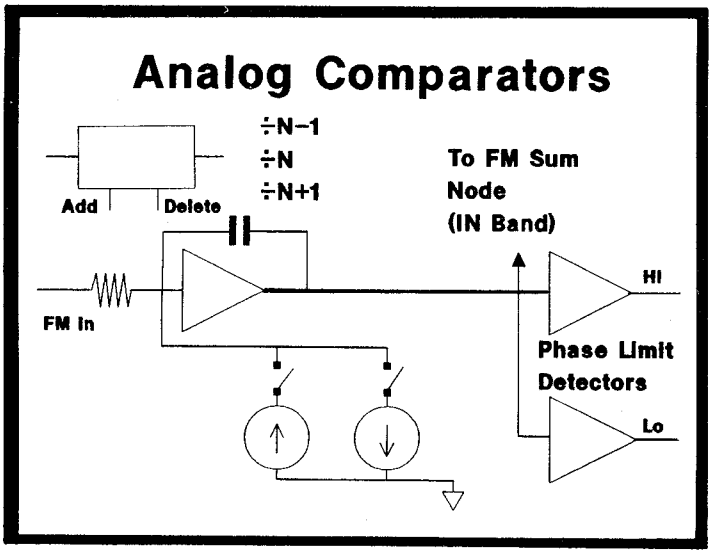


1191
The sensitivity of the phase node is multiplied by N. Compensation is needed as N changes. The summing node after the phase detector in the HP 8656B is really a current summing node. The current output of the FM integrator is sampled for a fixed number of VCO cycles. As the frequency goes up, N increases and the duty cycle of the sampler decreases. As the frequency goes down, the duty cycle goes up. The relationship is proportional to 1/N.

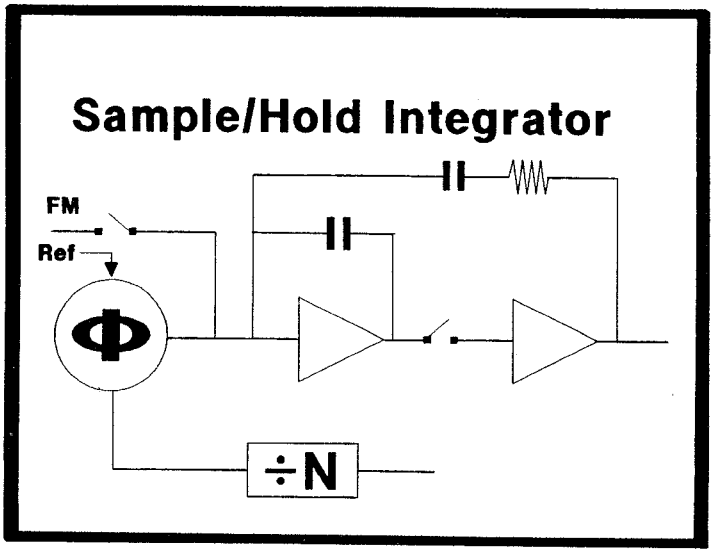


1192
The HP 8656B uses a prescaler in the FM Phase Locked Loop. It has the ability to divide by 9, 10, or 11. The normal mode is 10, and the 9 or 11 modes are used to add an extra cycle or delete one cycle from the overall divide number. This results in an added or subtracted two pi radians at the VCO.

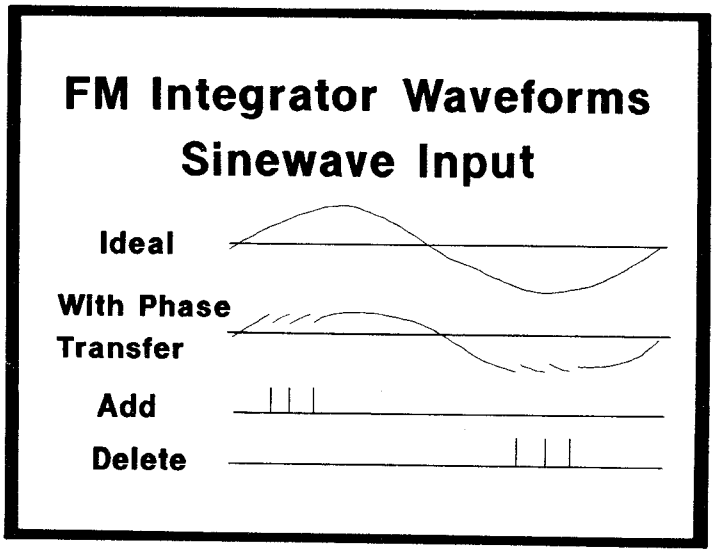




1193
The heart of the FM scheme is a transfer of phase offset from the FM integrator into the digital dividers inside the loop. This transfer is done in exact cycles added or removed. A current source is injected or removed from the input of the FM integrator for a controlled period to transfer the phase out of the integrator. Comparators are used to detect the output of the FM integrator (which is the instantaneous phase) to signal the need to reset the integrator.

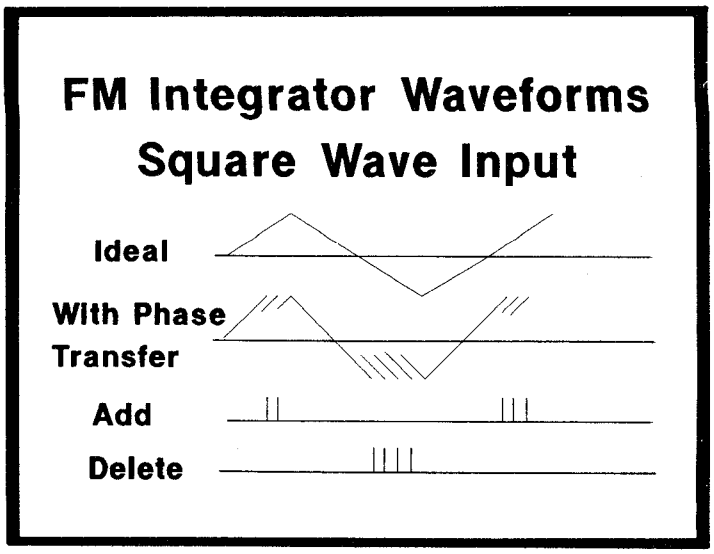


1194
Both the FM integrator reset and the divide number change need to happen during the same reference period. The timing diagram for controlling the loop allows integrator reset only when the sampler is off. In addition, there is a second integrator (part of the F(s) block) that allows the two events to settle so that the loop is not perturbed.

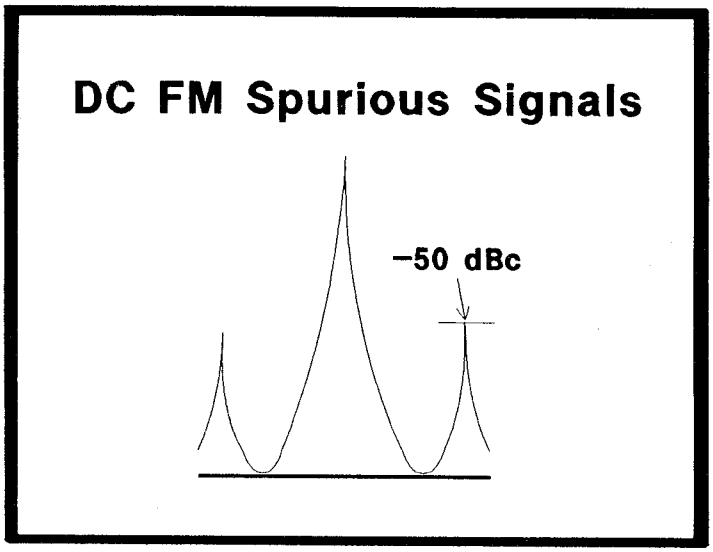


1195
The output of the FM integrator will have a response to various inputs that looks something like this:

1196
The output of the FM integrator will have a response to various inputs that looks something like this:



1197
Any inaccuracy in the reset of the integrator will result in a phase perturbation that is undesirable. If the resets are held to a constant rate (fixed DC deviation), then a discrete spurious will result. In the HP 8656B, the spurious level is better than −50 dBc. These spurious signals are attenuated by the PLL dynamics, which is an equivalent 2 kHz low pass filter. It should also be noted that sinusoidal FM signals result in a distributed spurious.



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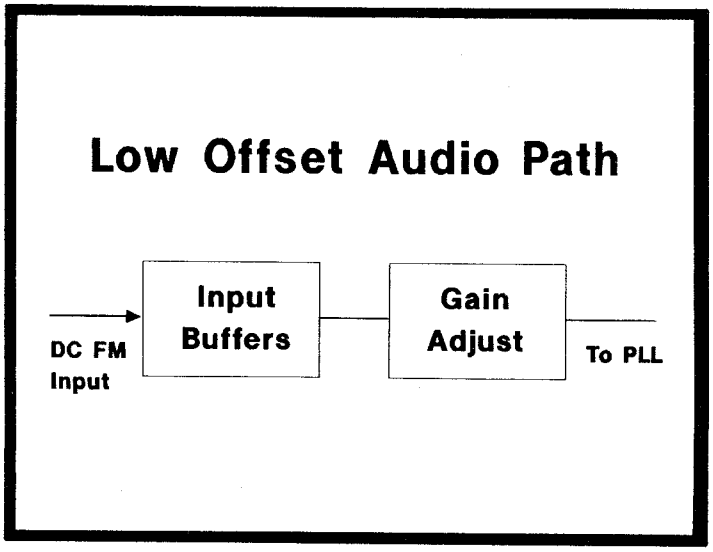
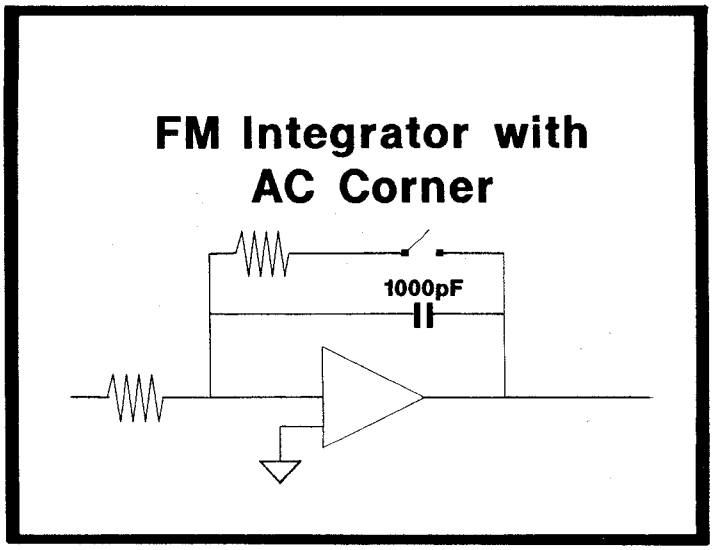
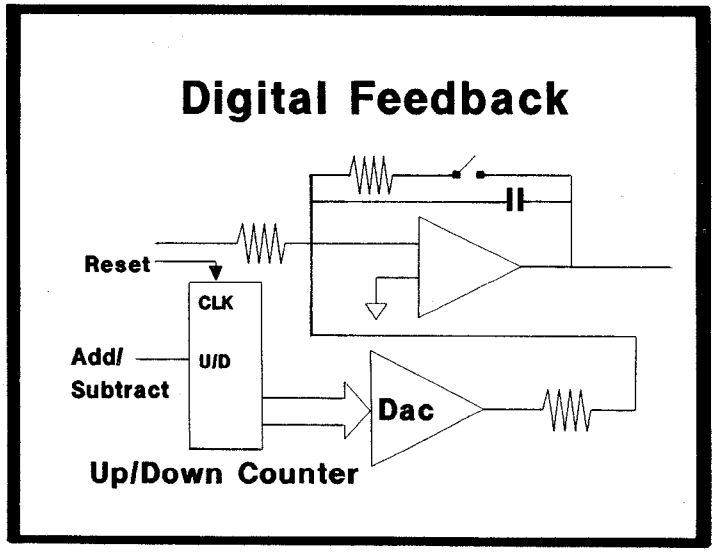
The DC FM performance of a phase locked loop with phase transfer is exceptional. Since the oscillator remains locked to the reference, the positive characteristics of the PLL are retained. These include the noise cleanup, and suppression of microphonics. In addition, the oscillator is not free running. It is locked to the reference; only the DC offsets at the FM integrator result in frequency error.



1199
Many customers need the frequency accuracy of a synthesizer when performing tests that do not require DC FM. AC FM needs to have synthesized center frequency for these tests. Any DC offset at the input of the FM integrator will result in a frequency error. Phase feedback is required to compensate for this effect. Phase feedback is achieved using a feedback resistor in the integrator and, in addition, using digital feedback.



1200
In the AC mode, the feedback current through the resistor should be proportional to the instantaneous phase offset. The steps in the output are lost current in the feedback path. To make up this lost current, a DAC has been added that has its LSB set to be the equivalent of one reset step on the output of the integrator. The counter is set to 50% when entering AC FM, and the DAC is offset so that there is no extra feedback current.



1201
The result of the digital FM technologies developed for the HP 8656B is a new standard for FM performance. AC FM has retained high performance and the DC coupled FM has achieved better stability than ever before.