HEWLETT hp PACKARD

COMPONENTS

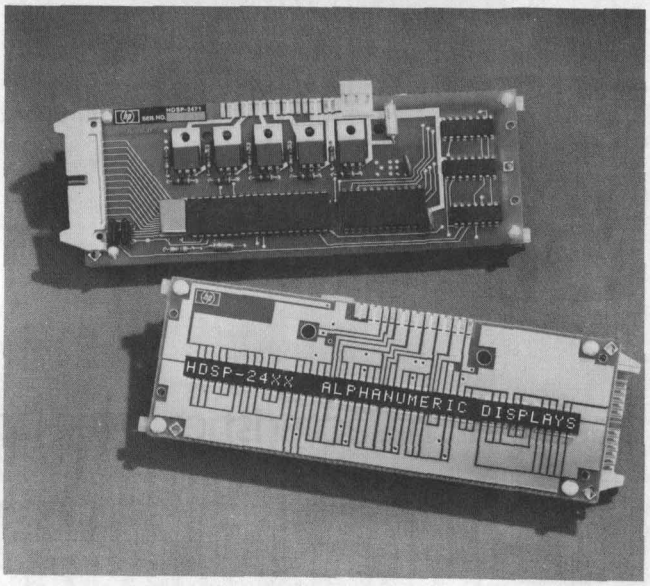
5 x 7 DOT MATRIX ALPHANUMERIC DISPLAY SYSTEM

HDSP - 2416
HDSP - 2424
HDSP - 2432
HDSP - 2440
HDSP - 2470
HDSP - 2471
HDSP - 2472

TENTATIVE DATA SEPTEMBER 1978

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-2000 DISPLAY**
- **CHOICE OF 64, 128, OR USER DEFINED ASCII CHARACTER SET**
- **CHOICE OF 16, 24, 32, or 40 ELEMENT DISPLAY PANEL**
- **MULTIPLE DATA ENTRY FORMATS — Left, Right, RAM, or Block Entry**
- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, AND CLEAR**
- **DATA OUTPUT CAPABILITY**
- **SINGLE 5.0 VOLT POWER SUPPLY**
- **TTL COMPATIBLE**
- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**



Description

The HDSP-24XX series of alphanumeric display systems provides the user with a completely supported 5 x 7 dot matrix display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays. Each alphanumeric display system is composed of two component parts:

1. An alphanumeric display controller which consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-2000 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines.
2. A display panel which consists of HDSP-2000 displays matched for luminous intensity and mounted on a P.C. board designed to have low thermal resistance.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation, electronic typewriters, and other products which require an easy to use 5 x 7 dot matrix alphanumeric display system.

PART NUMBER	DESCRIPTION
Display Boards	
HDSP-2416	Single-line 16 character display panel utilizing the HDSP-2000 display
HDSP-2424	Single-line 24 character display panel utilizing the HDSP-2000 display
HDSP-2432	Single-line 32 character display panel utilizing the HDSP-2000 display
HDSP-2440	Single-line 40 character display panel utilizing the HDSP-2000 display
Controller Boards	
HDSP-2470	HDSP-2000 display interface incorporating a 64 character ASCII decoder
HDSP-2471	HDSP-2000 display interface incorporating a 128 character ASCII decoder
HDSP-2472	HDSP-2000 display interface without ASCII decoder. Instead, a 24 pin socket is provided to accept a custom 128 character set from a user programmed 1K x 8 PROM.

When ordering, specify one each of the Controller Board and the Display Board for each complete system.

Absolute Maximum Ratings

V_{CC} ..... -0.5V to 6.0V

Operating Temperature Range, Ambient (T_A) ..... 0°C to 70°C

Storage Temperature Range (T_S) .... -55°C to 100°C

Voltage Applied to any Input or Output ..-0.5V to 6.0V

I_{SOURCE} Continuous for any Column Driver ..... 5.0 Amps (60 sec. max. duration)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out	I_{OL}		0.4	mA
	I_{OH}		-20	μA
Ready, Data Valid, Column On, Display Data	I_{OL}		1.6	mA
	I_{OH}		-40	μA
Clock	I_{OL}		10.0	mA
	I_{OH}		-1.0	mA
$Column_{1-5}$	I_{SOURCE}		-5.0	A

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Supply Current[1]	I_{CC}			400	mA	V_{CC} = 5.25V Column On and All Outputs Open	
Input Threshold High (except Reset)	V_{IH}	2.0			V	V_{CC} = 5.0V ± .25V	
Input Threshold High — Reset[2]	V_{IH}	3.0			V	V_{CC} = 5.0V ± .25V	
Input Threshold Low — All Inputs	V_{IL}			0.8	V	V_{CC} = 5.0V ± .25V	
Data Out Voltage	V_{OH}Data	2.4			V	I_{OH} = -20μA	V_{CC} = 4.75V
	V_{OL}Data			0.5	V	I_{OL} = 0.4mA	V_{CC} = 4.75V
Clock Output Voltage	V_{OH}Clk	2.4			V	I_{OH} = -1000μA	V_{CC} = 4.75V
	V_{OL}Clk			0.5	V	I_{OL} = 10.0mA	V_{CC} = 4.75V
Ready, Display Data, Data Valid, Column on Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA	V_{CC} = 4.75V
	V_{OL}			0.5	V	I_{OL} = 1.6mA	V_{CC} = 4.75V
Input Current,[3] All Inputs Except Reset, Chip Select, D_7	I_{IH}			-0.3	mA	V_{IH} = 2.4V	V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V	V_{CC} = 5.25V
$\overline{\text{Reset}}$ Input Current	I_{IH}			-0.3	mA	V_{IH} = 3.0V	V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V	V_{CC} = 5.25V
Chip Select, D_7 Input Current	I_I	-10		+10	μA	0 < V_I < V_{CC}	
Column Output Voltage	V_{OL}COL	2.6	3.2		V	I_{OUT} = -5.0A	V_{CC} = 5.00V

NOTES:

1. See Figure 11 for total system supply current.
2. External reset may be initiated by grounding Reset with either a switch or TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/s.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-2470/1/2.

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... -0.5V to 6.0V
Inputs, Data Out and V_B ..... -0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... -0.5V to +6.0V
Free Air Operating Temperature Range, T_A[1] ..... 0°C to +55°C
Storage Temperature Range, T_S .... -55°C to +100°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Norm.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Column Input Voltage, Column On	V_{COL}	2.6			V
Setup Time	t_{SETUP}	70	45		ns
Hold Time	t_{HOLD}	30	0		ns
Width of Clock	$t_{W(CLOCK)}$	75			ns
Clock Frequency	f_{CLOCK}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating[1] Temperature Range	T_A	0		55	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.*	Max.	Units	Conditions	
Supply Current		I_{CC}		45n	60n[2]	mA	V_{CC} = 5.25V, V_{CLOCK}=V_{DATA}=2.4V, All SR Stages = Logical 1	V_B = 0.4V
				73n	95n	mA		V_B = 2.4V
Column Current at any Column Input		I_{COL}			1.5n	mA	V_{CC} = V_{COL} = 5.25V, All SR Stages = Logical 1	V_B = 0.4V
		I_{COL}		335n	410n	mA		V_B = 2.4V
Peak Luminous Intensity per LED (Character Average)		$I_{V\ PEAK}$	105	200		μcd	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[3], V_B = 2.4V	
V_B, Clock or Data Input Threshold High		V_{IH}	2.0			V	V_{CC} = V_{COL} = 4.75V	
V_B, Clock or Data Input Threshold Low		V_{IL}			0.8	V		
Input Current Logical 1	V_B, Clock	I_{IH}			80	μA	V_{CC} = 5.25V, V_{IH} = 2.4V	
	Data In	I_{IH}			40	μA		
Input Current Logical 0	V_B, Clock	I_{IL}		-500	-800	μA	V_{CC} = 5.25V, V_{IL} = 0.4V	
	Data In	I_{IL}		-250	-400	μA		
Power Dissipation Per Board[4]		P_D		0.66n		W	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LED's on per Character, V_B = 2.4V	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

NOTES:
1. Operation above 55°C (70°C MAX) may be achieved by the use of forced air (150 fpm normal to component side of HDSP-247X controller board at sea level).
2. n = number of HDSP-2000 packages
   HDSP-2416 n = 4
   HDSP-2424 n = 6
   HDSP-2432 n = 8
   HDSP-2440 n = 10
3. Tj refers to initial case temperature immediately prior to the light measurement.
4. Power dissipation with all characters illuminated.

System Overview

The HDSP-2470/-2471/-2472 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-2000 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system refreshes HDSP-2000 displays from 4 to 48 characters with the decoded data.

The user interfaces to any of the systems through eight DATA IN inputs, five ADDRESS inputs (RAM mode), a CHIP SELECT input, RESET input, seven DATA OUT outputs, a READY output, DATA VALID output, and a COLUMN ON output. A low level on the RESET input clears the display and initializes the system. A low level on the CHIP SELECT input causes the system to load data from the DATA IN and ADDRESS inputs into the system. The controller outputs a status word, cursor address and 32 ASCII data characters through the DATA OUT outputs and DATA VALID output during the time the system is waiting to refresh the next column of the display. The COLUMN ON output can be used to synchronize the DATA OUT function. A block diagram for the HDSP-2470/-2471/-2472 systems is shown in Figure 1.

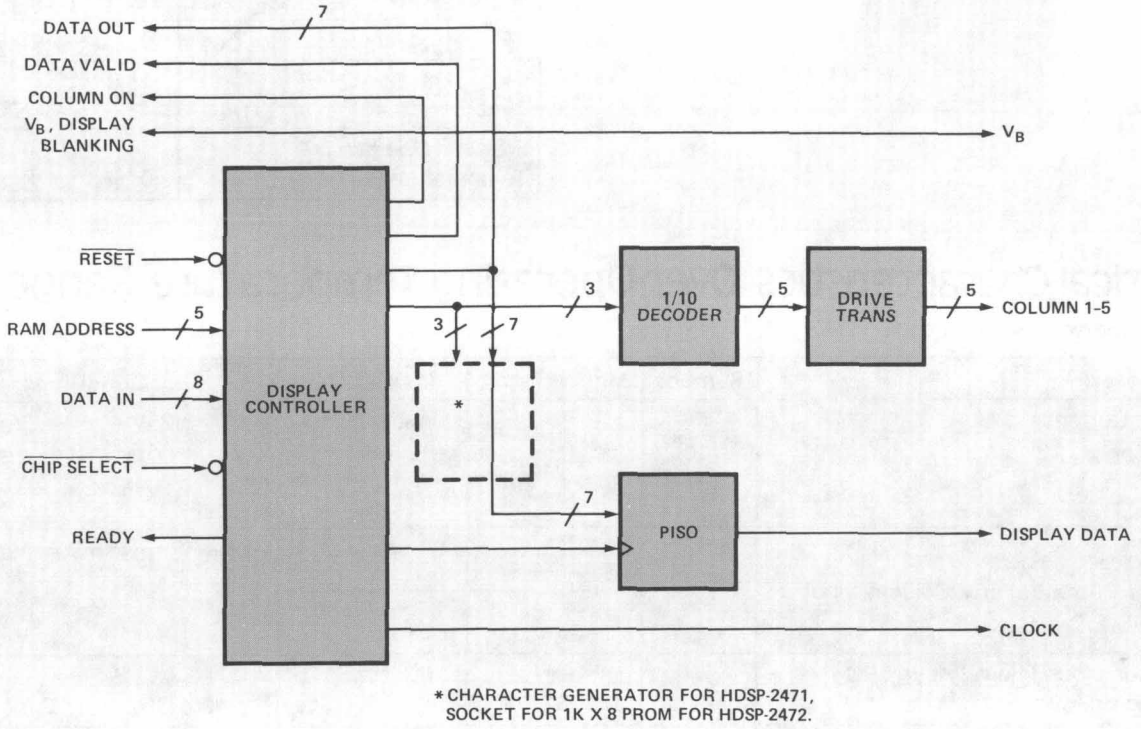


Figure 1. Block Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

The system interfaces to the HDSP-2000 display through five COLUMN outputs, a CLOCK output, DISPLAY DATA output, and the COLUMN ON output. The user should connect DISPLAY DATA to DATA IN of the leftmost HDSP-2000 cluster and cascade DATA OUT to DATA IN of all HDSP-2000 clusters. COLUMN outputs from the system are connected to the COLUMN inputs of all HDSP-2000 clusters. The HDSP-24XX Series display boards are designed to interconnect directly with the HDSP-247X Series display controllers. The COLUMN outputs can source enough current to drive up to 48 characters of the HDSP-2000 display. Pulse width modulation of display luminous intensity can be provided by connecting COLUMN ON to the input of a monostable multivibrator and the output of the monostable multivibrator to the V_B inputs of the HDSP-2000 displays. The system is designed to refresh the display at a fixed refresh rate of 100 Hz. COLUMN ON time is optimized for each display length in order to maximize light output as shown in Figure 2.

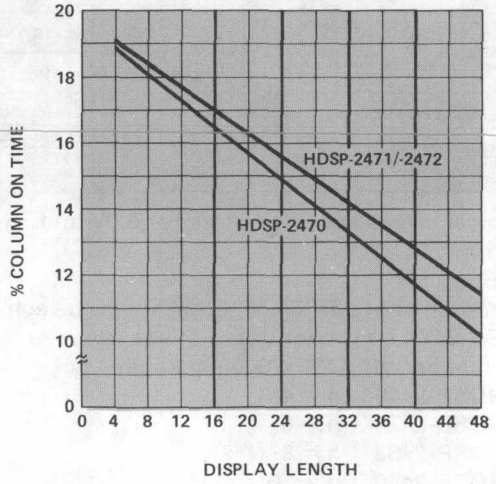


Figure 2. Column on Time vs. Display Length for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Control Mode/Data Entry

User interface to the HDSP-247X Series controller is via an 8 bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8 bit word, two additional control lines, CHIP SELECT and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the CHIP SELECT input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and the number of alphanumeric characters to be displayed.

The 8 bit control data word format is outlined in Figure 3. For the control word (D_7 high), bits D_6 and D_5 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_4 is ignored.

Control word inputs are first checked to verify that the control word is valid. The system ignores display lengths greater than 1011 for left block or right, or 0111 for RAM. If the word is valid, the present state—next state table shown in Figure 4 is utilized to determine whether or not to clear the display. For display lengths of up to 32 characters, RAM entry can be used as a powerful editing tool, or can be used to preload the cursor. With other transitions, the internal data memory is cleared.

CONTROL WORD: $D_7D_6D_5D_4D_3D_2D_1D_0$

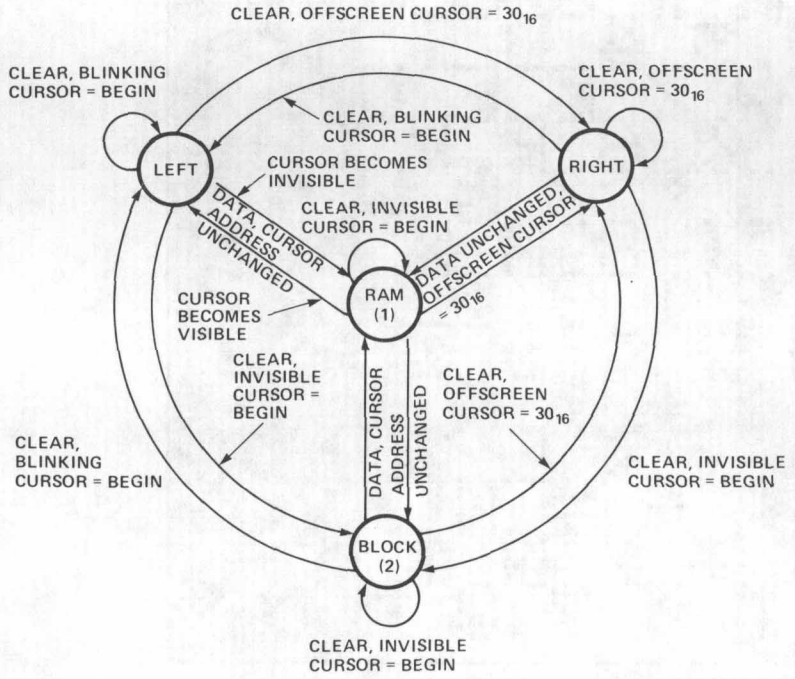
1	X	X	–	Y	Y	Y	Y

Y Y Y Y	DISPLAY LENGTH:
0 0 0 0	4 DIGITS
0 0 0 1	8 "
0 0 1 0	12 "
0 0 1 1	16 "
0 1 0 0	20 "
0 1 0 1	24 "
0 1 1 0	28 "
0 1 1 1	32* "
1 0 0 0	36 "
1 0 0 1	40 "
1 0 1 0	44 "
1 0 1 1	48 "

*maximum for RAM data entry mode

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Figure 3. Control Word Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



(1) RAM ENTRY MODE IS VALID FOR DISPLAYS OF 32 CHARACTERS OR LESS IN LENGTH.
(2) FOLLOWING A TRANSITION FROM RAM TO BLOCK, WHEN THE CURSOR ADDRESS IS 48 (30_{16}) DURING THE TRANSITION, THE FIRST VALID ASCII CHARACTER WILL BE IGNORED AND THE SECOND VALID ASCII CHARACTER WILL BE LOADED IN THE LEFT-MOST DISPLAY LOCATION.

WHERE BEGIN IS DEFINED AS FOLLOWS:

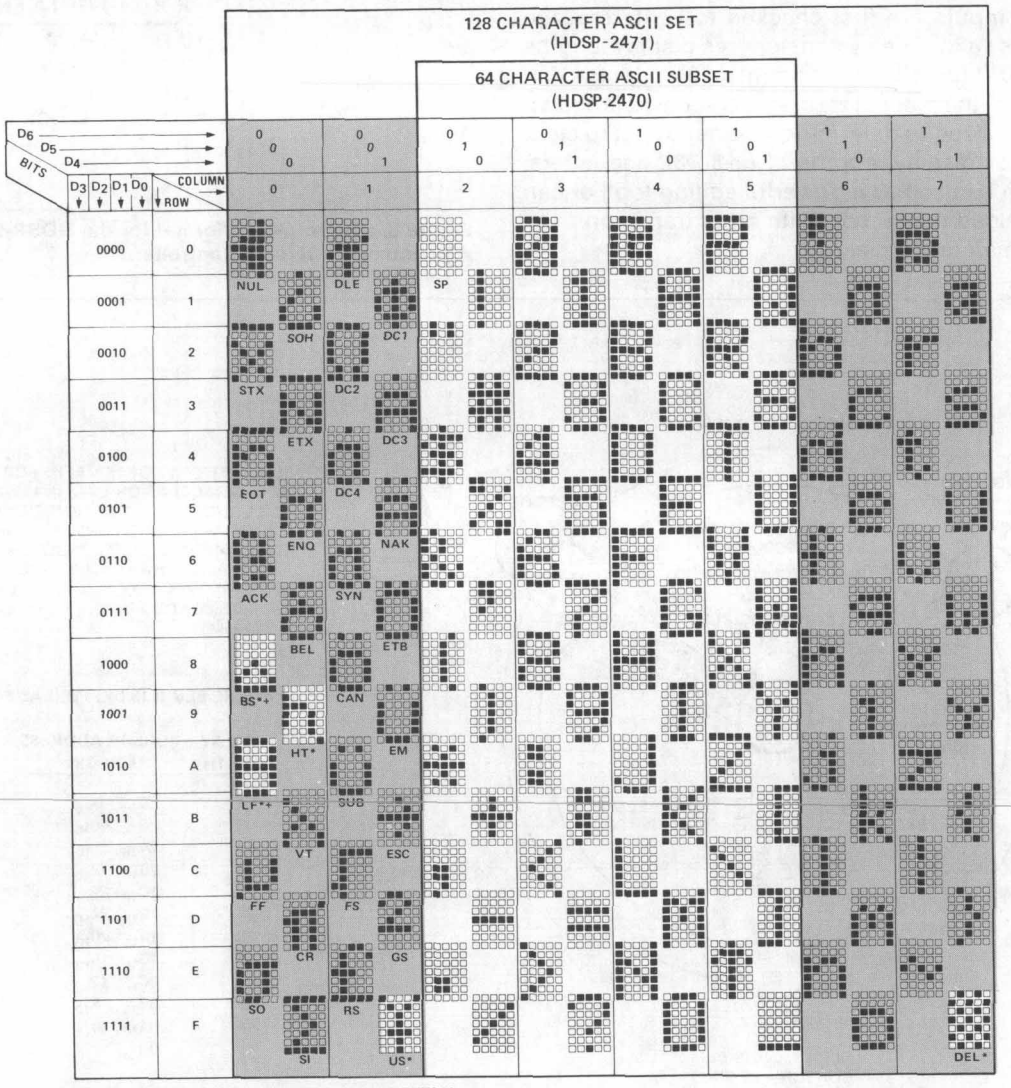
DISPLAY LENGTH	CURSOR ADDRESS OF BEGIN
4	$2C_{16}$, 44_{10}
8	28_{16}, 40_{10}
12	24_{16}, 36_{10}
16	20_{16}, 32_{10}
20	$1C_{16}$, 28_{10}
24	18_{16}, 24_{10}
28	14_{16}, 20_{10}
32	10_{16}, 16_{10}
36	$0C_{16}$, 12_{10}
40	08_{16}, 8_{10}
44	04_{16}, 4_{10}
48	00_{16}

Figure 4. Present State-Next State Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded and displayed. The system accepts seven bit ASCII for all three versions. However, the HDSP-2470 system displays only the 64 character subset [20_{16} (space) to $5F_{16}$ (_)] and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 5. Displayed character sets for the HDSP-2470/-2471 systems are shown in Figure 6.

DATA WORD:	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
ASCII ASSIGNMENT	0	A	A	A	A	A	A	A	DISPLAY COMMAND	
LF		0	0	0	1	0	1	0	CLEAR	Valid in Right Entry Mode; Valid in Left Entry Mode
BS		0	0	0	1	0	0	0	BACKSPACE CURSOR	Valid in Right Entry Mode; Valid in Left Entry Mode
HT		0	0	0	1	0	0	1	FORWARDSPACE CURSOR	Valid in Left Entry Mode
US		0	0	1	1	1	1	1	INSERT CHARACTER	Valid in Left Entry Mode
DEL		1	1	1	1	1	1	1	DELETE CHARACTER	Valid in Left Entry Mode

Figure 5. Display Commands for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



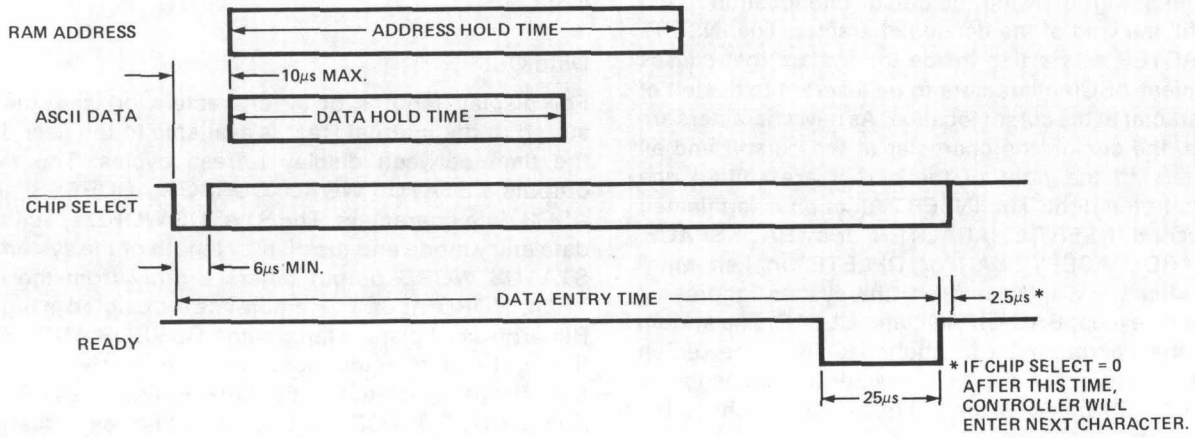
*DISPLAY COMMANDS WHEN USED IN LEFT ENTRY

+DISPLAY COMMANDS WHEN USED IN RIGHT ENTRY

Figure 6. Display Font for the HDSP-2470 (64 Character ASCII Subset), and HDSP-2471 (128 Character ASCII Set) Alphanumeric Display Controller.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 25μs and upon a positive transition, a new CHIP SELECT may be accepted by the controller. Data Entry Timing is shown in Figure 7.

DATA ENTRY TIMING



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE			FUNCTION					
HDSP-	DATA HOLD TIME*		DATA ENTRY	BACK SPACE	CLEAR	FORWARD SPACE	DELETE	INSERT
LEFT (2471/2)	135μs		235μs	195μs	505μs	205μs	725μs	725μs
LEFT (2470)	150μs		245μs	215μs	530μs	225μs	745μs	735μs
RIGHT (2471/2)	85μs		480μs	470μs	465μs			
RIGHT (2470)	105μs		490μs	490μs	485μs			
RAM (2471/2)	55μs	120μs**	190μs					
RAM (2470)	55μs	130μs**	200μs					
BLOCK (2471/2)	55μs		120μs	(155μs FOR RIGHTMOST CHARACTER)				
BLOCK (2470)	55μs		130μs	(165μs FOR RIGHTMOST CHARACTER)				
LOAD CONTROL (2471/2)	50μs		505μs					
LOAD CONTROL (2470)	50μs		505μs					

*Minimum time that data inputs must remain valid after Chip Select goes low.
**Minimum time that RAM address inputs must remain valid after Chip Select goes low.

Figure 7. Data Entry Timing and Data Entry Times for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forward space the cursor. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. FORWARDSPACE, INSERT, and DELETE have character assignments in this mode since they are not treated as editing characters. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a nonvisible cursor, the cursor is always loaded with the address of the next character to be entered. In this entry mode, the system can display the complete 128 character ASCII set. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the five bit RAM address. Due to the limitation of only five address lines, RAM data entry is allowed only for displays less than or equal to 32 characters. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. In RAM entry, the system can display the complete 128 character ASCII set because it does not interpret any of the characters as control functions. The display can be cleared by loading in a new RAM control word.

Data Out

For display lengths of 32 characters or less, the data stored in the internal RAM is available to the user during the time between display refresh cycles. The system outputs a STATUS WORD, CURSOR ADDRESS, and 32 ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD output differs slightly from the CONTROL WORD input. This difference is depicted in Figure 8. Regardless of display length, the CURSOR ADDRESS of the rightmost character location is address 47 ($2F_{16}$) and the offscreen address of the cursor is address 48 (30_{16}). The CURSOR ADDRESS of the leftmost location is defined as address 48 minus the display length. A general formula for CURSOR ADDRESS is:

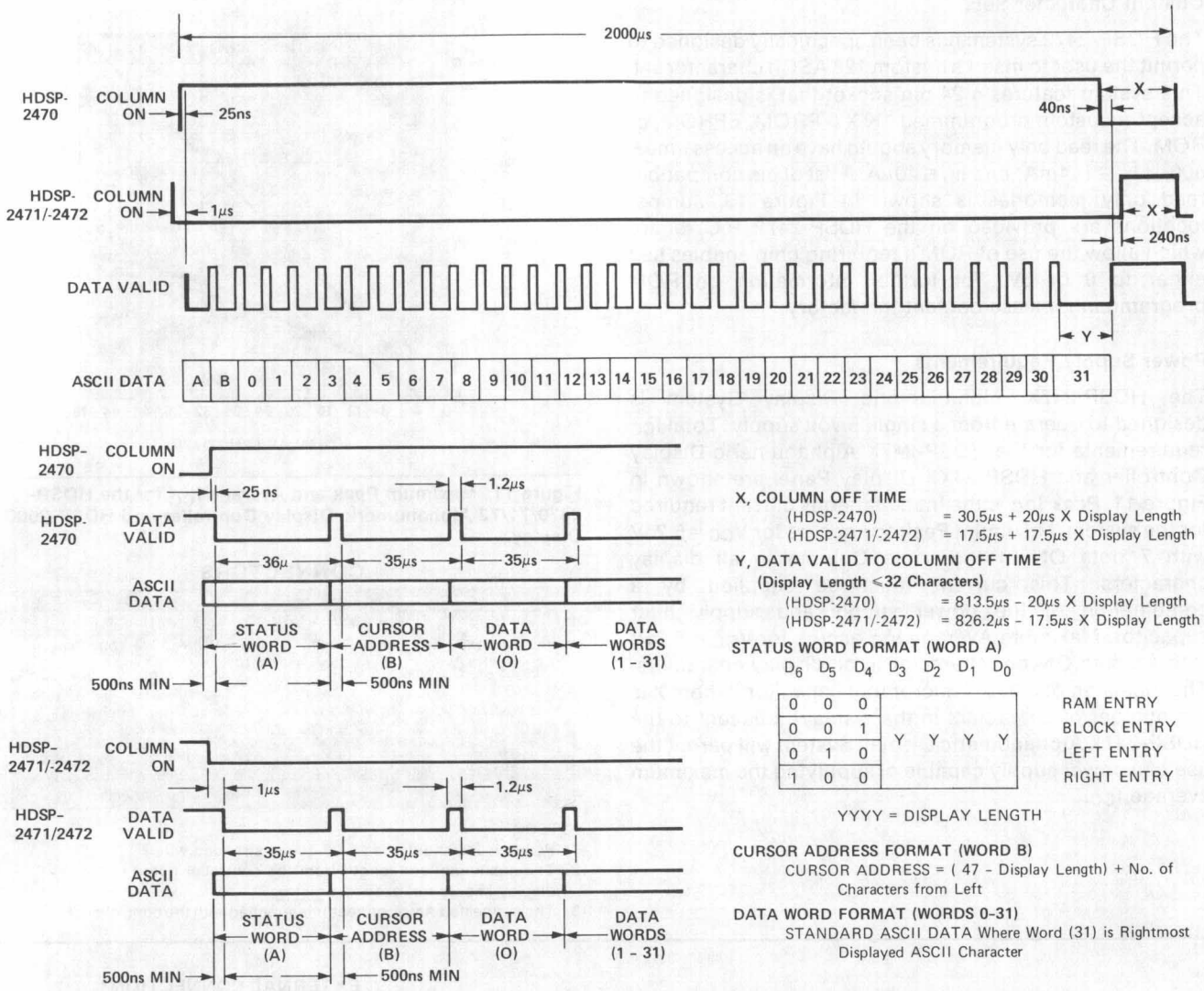
CURSOR ADDRESS =

(47 - Display Length) + Number of Characters from Left.

For example, suppose the alphanumeric display is 16 characters long and the cursor was blinking at the third digit from the left. Then the CURSOR ADDRESS would be 47 - 16 + 3 or 34 (22_{16}) and the 18th ASCII data word would correspond to the ASCII character at the location of the display cursor. In Left and Block entry, the CURSOR ADDRESS specifies the location where the next ASCII data character is to be entered. In RAM entry, the CURSOR ADDRESS specifies the location to the right of the last character entered. In Right entry, the CURSOR ADDRESS is always 48 (30_{16}). The negative edge of the DATA VALID output can be used to load the 34 DATA OUT words into the user's system. The DATA OUT timing for the HDSP-247X systems are summarized in Figure 8. For displays longer than 32 characters, the system only outputs the STATUS WORD between refresh cycles.

Master/Power On Reset

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the systems loads the control word on the DATA INPUTS into the system. If $D_7 \leq .8V$ or the system sees an invalid control word, the system initializes as Left entry for a 32 character display with a flashing cursor in the leftmost location. For POWER ON RESET to function properly, the power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the RESET input low for a minimum of 50 milliseconds. POWER ON/MASTER RESET timing is shown in Figure 9.



X, COLUMN OFF TIME

(HDSP-2470) = 30.5µs + 20µs X Display Length

(HDSP-2471/-2472) = 17.5µs + 17.5µs X Display Length

Y, DATA VALID TO COLUMN OFF TIME

(Display Length ≤32 Characters)

(HDSP-2470) = 813.5µs - 20µs X Display Length

(HDSP-2471/-2472) = 826.2µs - 17.5µs X Display Length

STATUS WORD FORMAT (WORD A)

D_6 D_5 D_4 D_3 D_2 D_1 D_0

0	0	0	Y	Y	Y	Y	RAM ENTRY
0	0	1					BLOCK ENTRY
0	1	0					LEFT ENTRY
1	0	0					RIGHT ENTRY

YYYY = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (WORD B)

CURSOR ADDRESS = (47 - Display Length) + No. of Characters from Left

DATA WORD FORMAT (WORDS 0-31)

STANDARD ASCII DATA Where Word (31) is Rightmost Displayed ASCII Character

Figure 8. Data Out Timing and Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

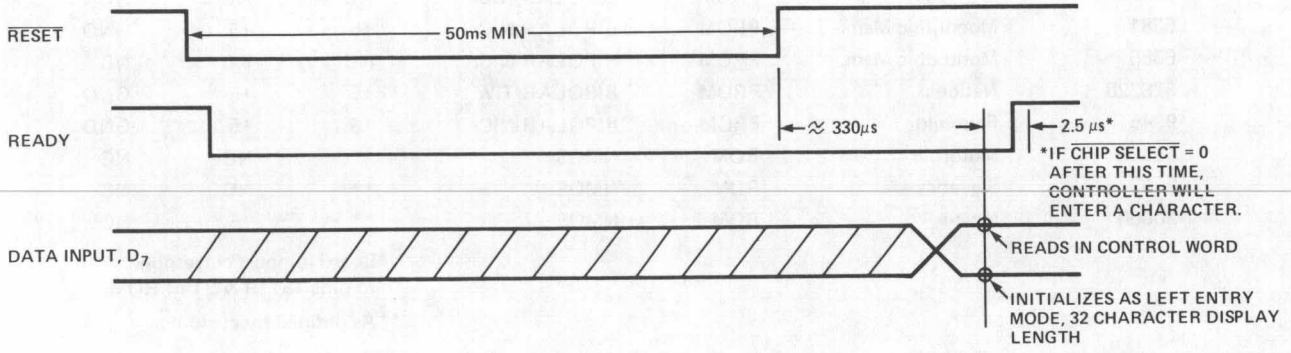


Figure 9. Power-On/Master Reset Timing for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Custom Character Sets

The HDSP-2472 system has been specifically designed to permit the user to insert a custom 128 ASCII character set. This system features a 24 pin socket that is designed to accept a custom programmed 1K X 8 PROM, EPROM, or ROM. The read only memory should have an access time $\leq$ 500ns, $I_{IL} \leq |-.4mA|$ and $I_{IH} \leq 40\mu A$. A list of pin compatible read only memories is shown in Figure 10. Jumper locations are provided on the HDSP-2472 P.C. board which allow the use of ROM's requiring chip enables tied either to 0 or 5V. For further information on ROM programming, please contact the factory.

Power Supply Requirements

The HDSP-247X Alphanumeric Display System is designed to operate from a single 5 volt supply. Total I_{CC} requirements for the HDSP-247X Alphanumeric Display Controller and HDSP-24XX Display Panel are shown in Figure 11. Peak I_{CC} is the instantaneous current required for the system. Maximum Peak I_{CC} occurs for $V_{CC} = 5.25V$ with 7 dots ON in the same Column in all display characters. This current must be supplied by a combination of the power supply and supply filter capacitor. Maximum Average I_{CC} occurs for $V_{CC} = 5.25V$ with 21 dots ON per character in all display characters. The inclusion of a 375 X microfarad capacitor (where X is the number of characters in the display) adjacent to the HDSP-247X Alphanumeric Display System will permit the use of a power supply capable of supplying the maximum average I_{CC}.

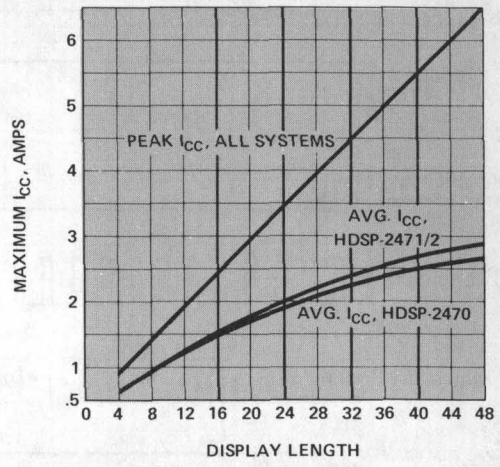


Figure 11. Maximum Peak and Average I_{CC} for the HDSP-2470/71/72 Alphanumeric Display Controller and HDSP-2000 Display.

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	26 Pin Ribbon Cable	3M P/N 3399-X000 Series
POWER(1)	3 Pin With Locking Ramp	Molex P/N 09-50-3031 with 08-50-0106 Terminals
DISPLAY DRIVE(2,3)	17 Lead Board to Board	Amp P/N 1-530500-7, also available in board to cable and other configurations

NOTES:
(1) Power leads should be 18-20 gauge stranded wire.
(2) The maximum lead length from the controller board to the display should not exceed 1 metre.
(3) The suggested Amp connector is supplied with the controller.

PART NUMBER	MANUFACTURER	TYPE	CONSTRUCTION	EXTERNAL CONNECTION* X	Y	Z
2758	Intel	EPROM	NMOS	GND	GND	+5
7608	Harris	PROM	BIPOLAR-NiCr	NC	NC	NC
3628-4	Intel	PROM	BIPOLAR-Si	+5	+5	GND
82S2708	Signetics	PROM	BIPOLAR-NiCr	NC	NC	NC
6381	Monolithic Mem.	PROM	BIPOLAR-NiCr	+5	+5	GND
6385	Monolithic Mem.	PROM	BIPOLAR-NiCr	NC	NC	NC
87S228	National	PROM	BIPOLAR-TiW	+5	+5	GND
93451	Fairchild	PROM	BIPOLAR-NiCr	+5	+5	GND
68308	Motorola	ROM	NMOS	**	NC	NC
2607	Signetics	ROM	NMOS	**	NC	NC
30000	Mostek	ROM	NMOS	**	+5	NC

*Board jumpers correspond to pins 18, 19 & 21 of ROM.

**As defined by customer

Figure 10. Pin Compatible 1K x 8 Read Only Memories for the HDSP-2472 Alphanumeric Display Controller.

Display Boards/Hardware

The mechanical layout of the HDSP-247X Series allows direct mating of the controller P.C. board to a compatible series of display boards available from Hewlett-Packard. These display boards consist of matched and tested HDSP-2000 clusters soldered to a P.C. board.

Included with the controller board are: 1 each Amp P/N 1-530500-7 board to board connector, and 4 each locking circuit board support nylon standoffs (Richco LCBS-4). This hardware allows the controller board to interconnect with any of the standard display boards. Figure 12 depicts correct assembly technique.

Assembly Steps

1. Insert the standoffs into .151 diameter holes (noted as "S" on Figure 12. The long end of the standoffs should protrude through the controller board side.
2. Position the controller board and display board with the components and displays facing out. The HP logo should be in the upper left corner when viewed facing the boards. Insert the standoffs through the mating holes on the display board and press the boards together so that the standoffs lock in place.
3. After the standoffs are secured, the Amp connector should be placed on the edge connect pads (marked "A" through "Q" Figure 12) at the top of the boards. Visual alignment of this connector may be done on the controller board by determining that the first connector contact finger is centered on the pad labeled "A".

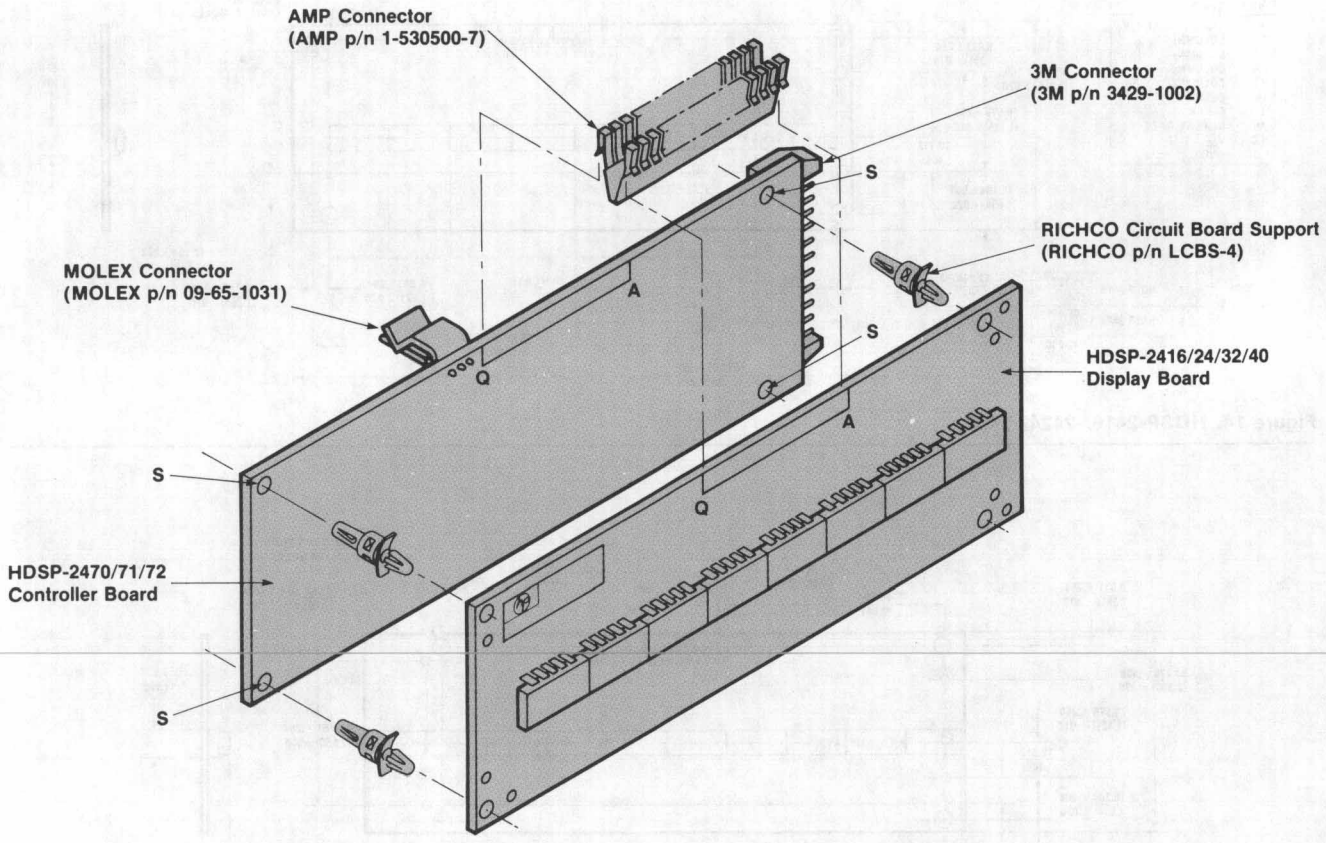


Figure 12. Assembly Drawing.

Package Dimensions

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN mm AND (INCHES)

HDSP-2470/-2471/-2472

PIN	DESCRIPTION
1	CHIP SELECT
2	DATA VALID
3	RAM ADDRESS, A_0
4	DATA IN, D_7
5	RAM ADDRESS, A_1
6	RESET
7	RAM ADDRESS, A_2
8	DATA OUT, DO_6
9	RAM ADDRESS, A_3
10	DATA OUT, DO_5
11	DATA IN, D_0
12	DATA OUT' DO_4
13	DATA IN, D_1
14	DATA OUT, DO_3
15	DATA IN, D_2
16	DATA OUT, DO_2
17	DATA IN, D_3
18	DATA OUT, DO_1
19	DATA IN, D_4
20	DATA OUT, DO_0
21	DATA IN, D_5
22	READY
23	DATA IN, D_6
24	COLUMN ON
25	RAM ADDRESS, A_4
26	DISPLAY BLANK, V_B

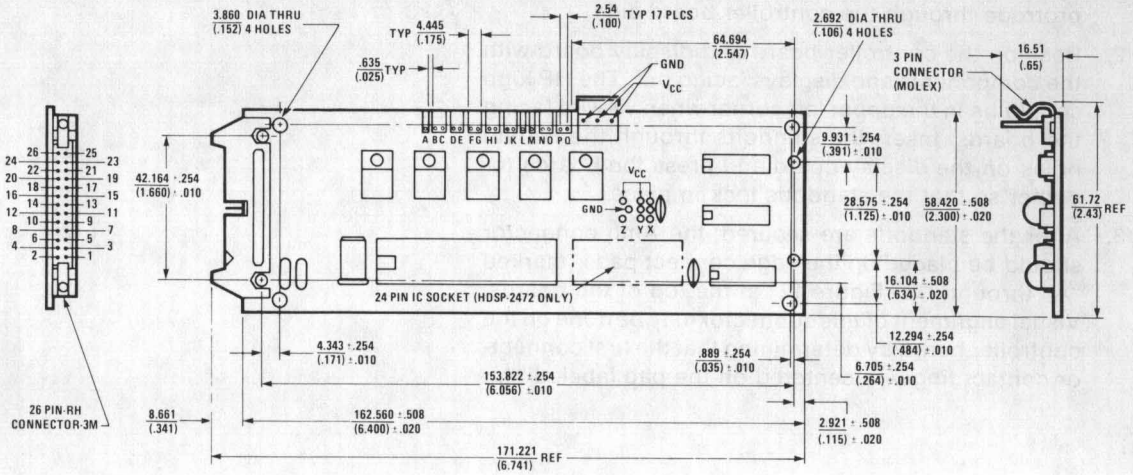


Figure 13. HDSP-2470/-2471/-2472

HDSP-2416/-2424/-2432/-2440
HDSP-2470/-2471/-2472

PIN	DESCRIPTION
A	DISPLAY BLANK, V_B
B,C	COLUMN$_1$
D,E	COLUMN$_2$
F,G	COLUMN$_3$
H,I	COLUMN$_4$
J,K	COLUMN$_5$
L	CLOCK
M	DISPLAY DATA
N,O	V_{CC}
P,Q	GND

A	HDSP-2416	71.120 (2.800)
B	HDSP-2424	106.680 (4.200)
C	HDSP-2432	142.240 (5.600)

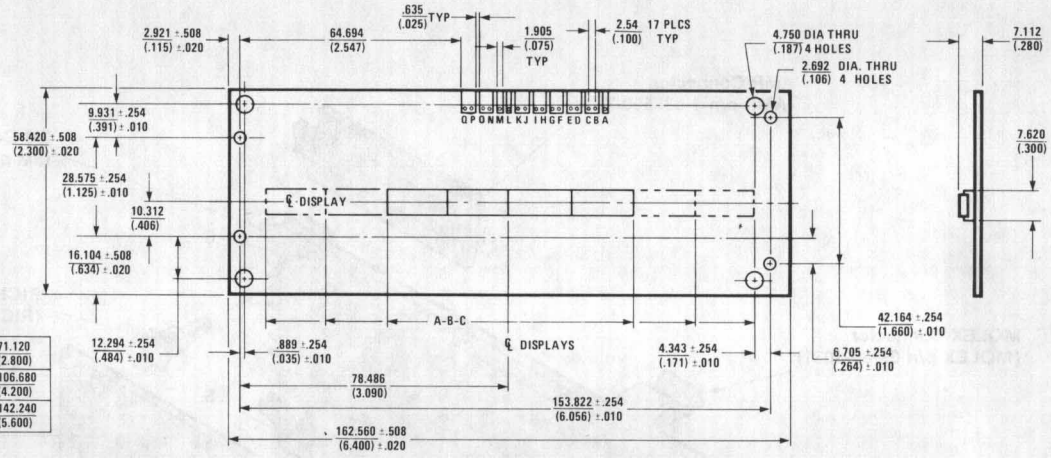


Figure 14. HDSP-2416/-2424/-2432

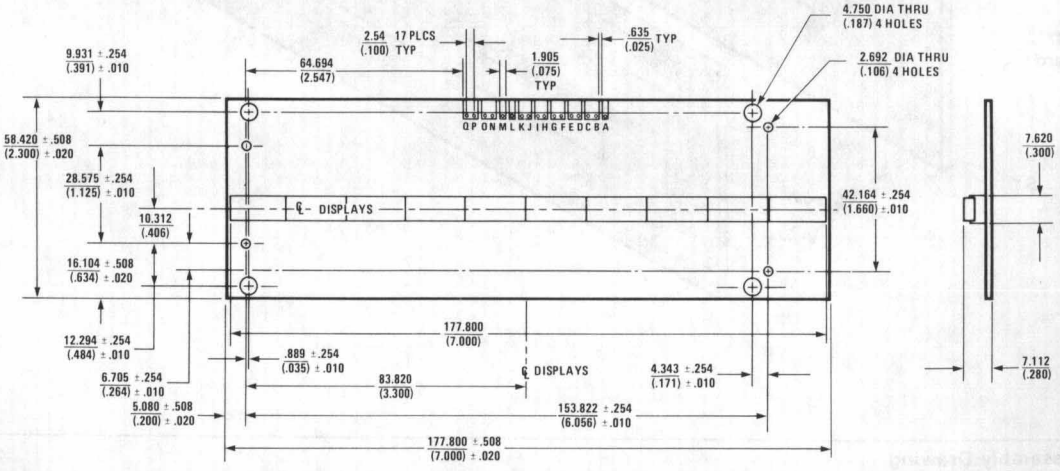


Figure 15. HDSP-2440