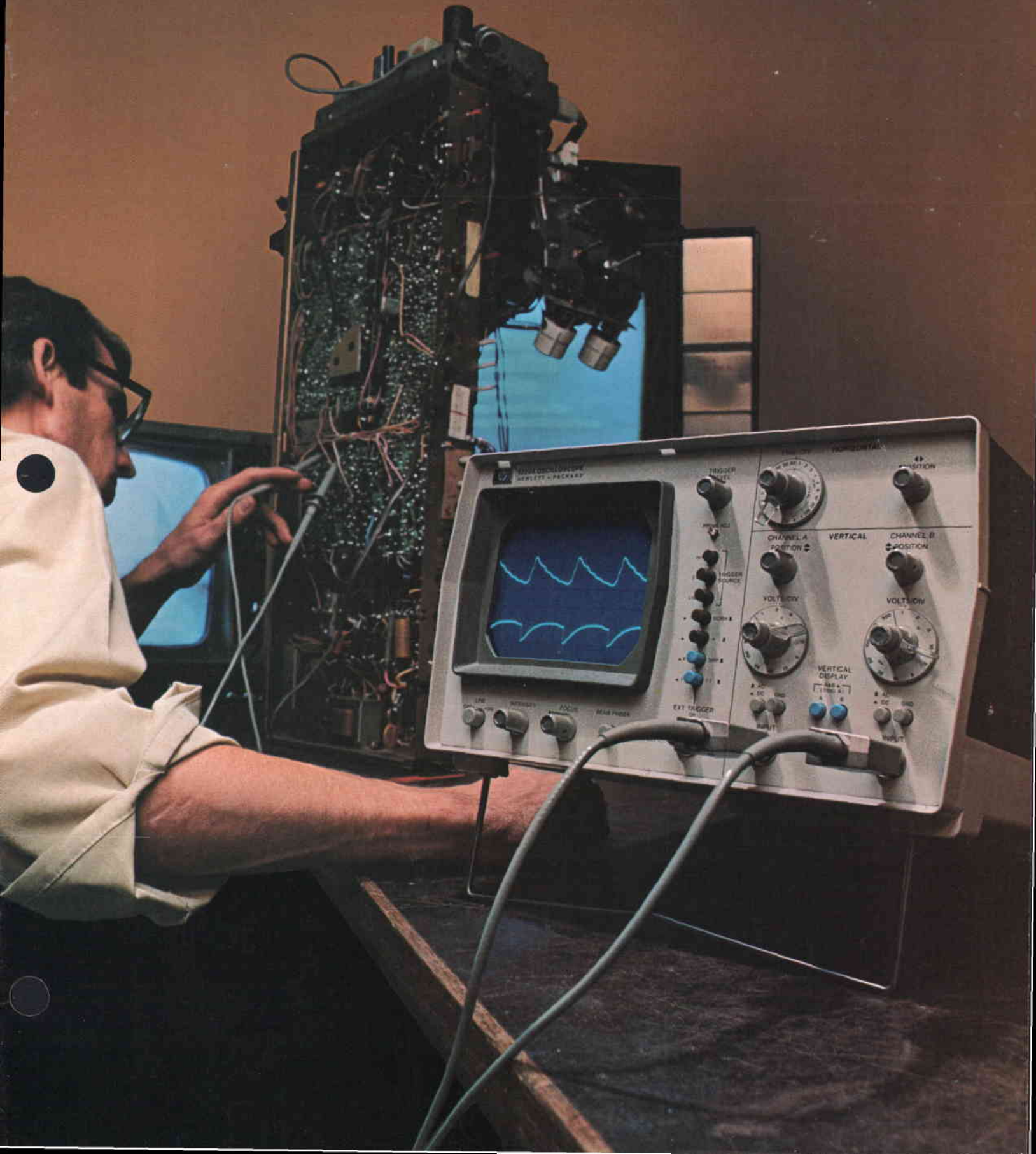


FEBRUARY 1974

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Practical Oscilloscopes at Workaday Prices

15-MHz bandwidth, 2mV sensitivity, 3% accuracy, sweeps usable to 20ns/div and an 8 × 10 cm CRT with internal graticule would normally class these oscilloscopes as laboratory instruments but they will find wide use in the service shop, technical school, and industry.

by Hans-Günter Hohmann

ADVANCES IN INSTRUMENTATION nowadays do not always involve the bettering of previous performance specifications but rather the bettering of performance/price ratios. Several new instruments recently described here—a counter¹, a digital voltmeter², and a function generator³—are of interest because their design made high-quality performance attainable for the technical school, service shop, and other low-budget operations, as well as for the well-equipped electronics laboratory.

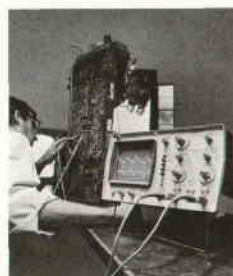
Now joining the family of instruments available for restricted budgets are two new oscilloscopes. With a frequency range of dc to 15 MHz, these belong among the basic tools for everyday work in the lab, service shop and production area. Advances in technology made it possible to design these instruments with a better performance/price ratio than would have been possible 5 or 6 years ago.

One of the new oscilloscopes, Model 1220A (Fig. 1), is a dual-channel instrument and the other, Model 1221A (Fig. 2), is a lower-cost, single channel version. These instruments have the performance needed for meeting a wide variety of applications (15 MHz bandwidth, 2 mV sensitivity, 3% accuracy, and calibrated sweep times from 0.5 s/div to 100 ns/div—even faster with the magnifier) and they have the most useful oscilloscope features (×10 sweep magnifier, beam finder, X-Y display capability, internal CRT graticule, TV sync separator). Above all, they have traditional HP reliability, and they have an affordable price.

Easy Operation

Despite the minimal cost, the new oscilloscopes have a number of operating conveniences that make them easy instruments to use. Considerable thought was devoted to achieving an uncluttered front-panel layout with controls placed so operation is easily understood. Automatic triggering assures that a base-

line is present even in the absence of a signal or if the trigger level control is set beyond the range of the signal. Although the dual-channel Model 1220A oscilloscope operates in either a chopped or an alternate sweep mode when displaying two signals, the operator need not concern himself with making the choice. The choice is made by the TIME/DIV switch, which selects the alternate-sweep mode (display channel A on one sweep then channel B on the next) when the sweep rate is fast enough to avoid flicker. On the slower sweeps, 1 ms/cm or longer, the switch selects the chopped mode (the CRT spot switches back and forth from one waveform to the other at a 200-kHz rate to trace both waveforms on the same



Cover: As new developments bring instrument costs down, TV service shops join the many other budget-restricted establishments that can now avail themselves of quality instruments, like the Model 1220A Oscilloscope described here. Our thanks to

Alco Home Electronics Service Center, Santa Clara, California, and to technician Jim Hagan for providing the setting for this photo.

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Fig. 1. New Model 1220A dual-channel Oscilloscope has performance and quality usually found only in laboratory instruments, yet it carries a down-to-earth price. Suitable for the general run of audio, video, logic, and control measurements, it can also make low-level measurements.

sweep). Similarly, when triggering from a TV signal, the sweep triggers on either the horizontal or the vertical sync pulses according to the setting of the TIME/DIV switch.

But even with their operating simplicity, the instruments have the flexibility needed for a wide range of applications. The operator can select the source of sweep triggers (internal, external, ac line, TV) and he can select the point on the waveform where he would want triggering to occur (slope, le-

vel). External signals can also be applied to the horizontal deflection amplifiers for making X-Y plots or the Lissajous figures commonly used for phase-shift measurements. There is also a rear-panel Z-axis input for modulating the CRT beam intensity.

These instruments also have reduced bulk and weight, weighing about 16 lbs (8 kg) each.

Reducing Costs

Obtaining reliability and versatility at low cost required some departures from traditional practice. A major expense in producing a complicated instrument like an oscilloscope is in assembly and test. The design of the new oscilloscopes eliminates several production steps both in fabricating parts and testing the circuits. For example, the cabinet is made of a molded, thermosetting resin (Fig. 3) that has a mechanical stability comparable to that of aluminum and that is widely used as a replacement for metal in automobiles and household appliances. It allows these oscilloscopes to be used in production areas, around process control equipment, and in other areas where ruggedness is needed. Because the cabinet can be molded in one operation with all mounting posts, bar stiffeners, access holes and the like in place, several manufacturing steps are eliminated. The cabinet is metallized on the inside surfaces where RF shielding is desired.

The internal chassis parts were designed in modular form for quick assembly by plugging together. This has the further advantage that the modules can



Fig. 2. Lower-priced Model 1221A Oscilloscope is identical to Model 1220A except that it has only one vertical channel.

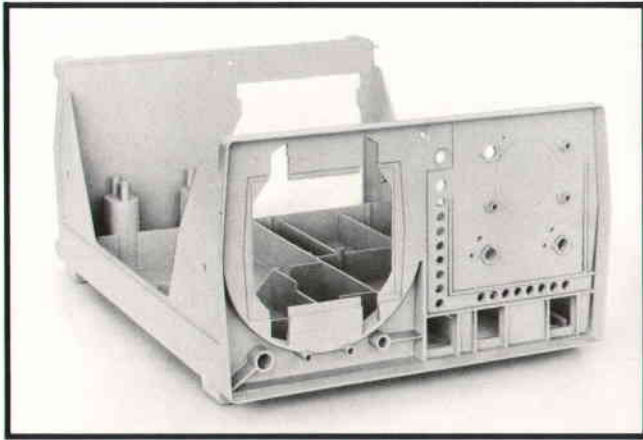


Fig. 3. The major structural component is molded with a thermosetting resin, greatly reducing the number of operations needed to manufacture the instrument.

be completely pre-tested by an automatic test system before final assembly. Most interconnections are made on printed-circuit boards with intermodule connections made by plug-in flat cables, significantly reducing wiring and assembly time.

In some cases, costs were reduced by using premium components rather than the least expensive. For example, precision resistors and capacitors are used in the sweep timing circuits. It was therefore not necessary to include the trimmers that otherwise would be needed had lower cost components with looser tolerances been used. Hence, no time is taken at the test station for adjusting those variable components that are no longer included.

Part of the cost reduction is simply a matter of advancing technology. High-performance solid-state components are now obtainable at lower prices and

the wide variety of available off-the-shelf integrated circuits make it possible to be almost extravagant in the use of functions. For instance, selection of most input sensitivity ranges is performed by switching the gain of the amplifiers. The input attenuator therefore needs only two positions and a straight-through position, reducing the number of adjustable frequency-compensating capacitors needed.

The Overview

A simplified block diagram of the new Model 1220A dual-channel oscilloscope is shown in Fig. 4. As can be seen, the general scheme of things is not much different from other dual-channel oscilloscopes. The Model 1221A single-channel version is similar except that it omits channel B and the circuits needed to multiplex two input channels into the single vertical CRT drive channel.

Solid-state circuits are used throughout. Power consumption is low, less than 40W, reducing internal heat rise with a consequent enhancement of reliability. No vent holes are needed, lessening the problems associated with operating in adverse environments.

The CRT

Although the design of any oscilloscope begins with the cathode-ray tube, the CRT design has to take into account the circuits that may be used. The Hewlett-Packard Model 1310A large-screen Graphic Display had shown that substantial drive voltages at high frequencies can be obtained at moderate cost from solid-state circuits.⁴ This meant that the expansion-mesh electrode—which had originally made high performance economically possible in all solid-state oscilloscope⁵—would not be needed for the new

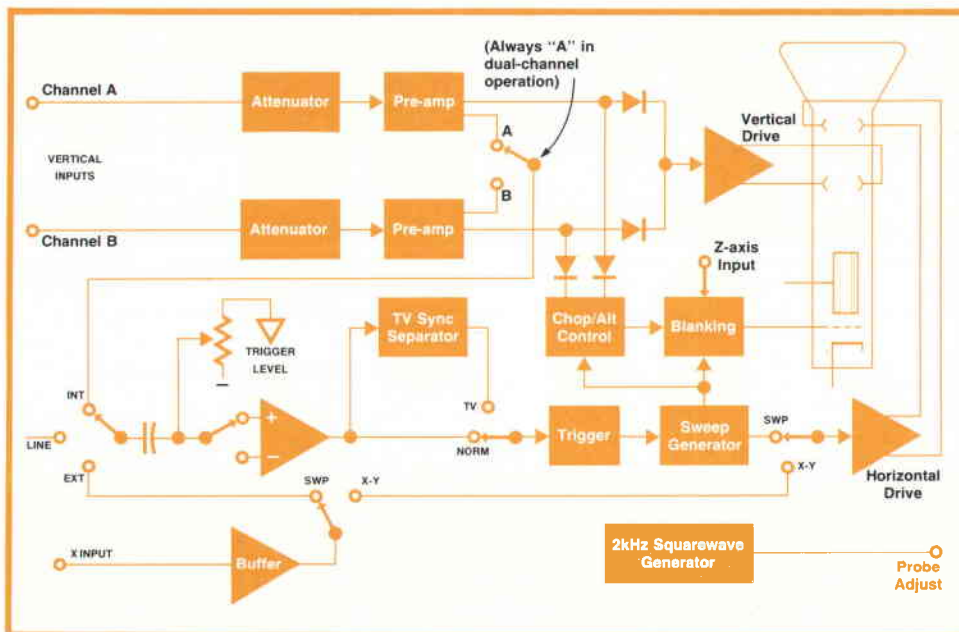


Fig. 4. Simplified block diagram of the Model 1220A Oscilloscope. The Model 1221A is similar except that it omits channel B and the chop/alt control.



Fig. 5. The cathode-ray tube for the new oscilloscopes uses an uncomplicated structure that reduces the number of manufacturing steps.

scopes. Furthermore, the drive voltage available meant that beam acceleration could be obtained entirely in the electron gun, and a post-accelerating field would not be needed. All this added up to a relatively simple structure that eliminated several processing steps.

One processing step that was not eliminated was insertion of the internal graticule. The black graticule lines are deposited on the inner surface of the faceplate and fused onto the faceplate before the phosphor (P31) is deposited, placing the graticule in the same plane as the phosphor. This eliminates the parallax errors that otherwise occur when the graticule is external to the CRT (Fig. 6). The improvement in reading accuracy is considered to be well worth the extra expense. Vertical deflection accuracy is within 3%, about as close as the eye can discern. This accuracy enables the oscilloscopes to be used as voltmeters as well as waveform tracers.

Gain Switching

A skeleton diagram of the input attenuator and first preamplifier stage is shown in Fig. 7. Input impedance on all ranges is 1 M Ω in parallel with 30 pF.

The input signal goes to a high-impedance FET stage that is part of a differential amplifier. The other input to the amplifier is a dc balance voltage. The two input FET's are mounted on the same substrate and thus have good thermal stability so once the balance voltage is set, it seldom needs readjustment. This made practical the instruments' high sensitivity (2mV/cm deflection factor).

The gain of the differential amplifier is changed by switching current sources Q5 and Q6. On the three most sensitive ranges, Q6 is turned on and Q5 off so emitter resistors R1 and R2 in parallel with R3 and R4 determine the gain of the amplifier. On all other ranges, Q5 is on and Q6 off so the smaller resistors are effectively cut out of the circuit by the decoupling diodes, reducing the amplifier gain by a factor of 10. As gain switching is performed by control voltages, the electrical and mechanical design could be simplified.

The output of the first stage passes through a second differential stage (not shown) that has adjustable feedback to calibrate the gain of the vertical amplifier. From there, the signal goes to another stage that uses three sets of switched emitter resistors to give gains proportional to $\times 1$, $\times 2$, and $\times 5$.

The signal then passes through a dc shifter to give vertical positioning control and a diode gate that multiplexes the two channels into a single channel (Fig. 4). The single channel goes to the CRT driver.

Economical Drive

One leg of the CRT driver stage is shown in Fig. 8. By dividing the 95V supply voltage across four transistors, lower-cost, low-voltage, high-frequency transistors may be used to obtain the 60V swing needed for each CRT deflection electrode.

The lower two transistors (Q10, Q11) are connected as a cascode amplifier for better high frequency response. The upper two (Q12, Q13), also in cascode, serve as a constant-current load for Q10 and

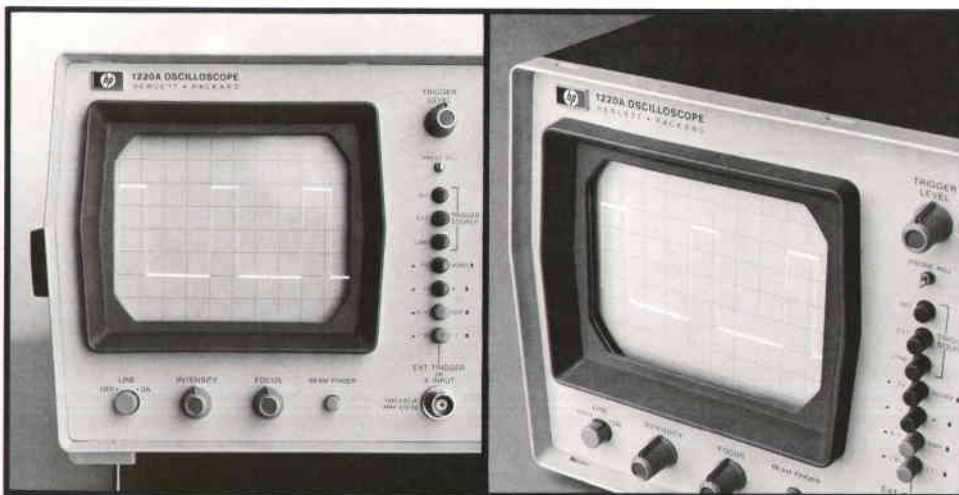


Fig. 6. Placing the CRT graticule in the same plane as the phosphor assures high measurement accuracy from any viewing angle by eliminating parallax.

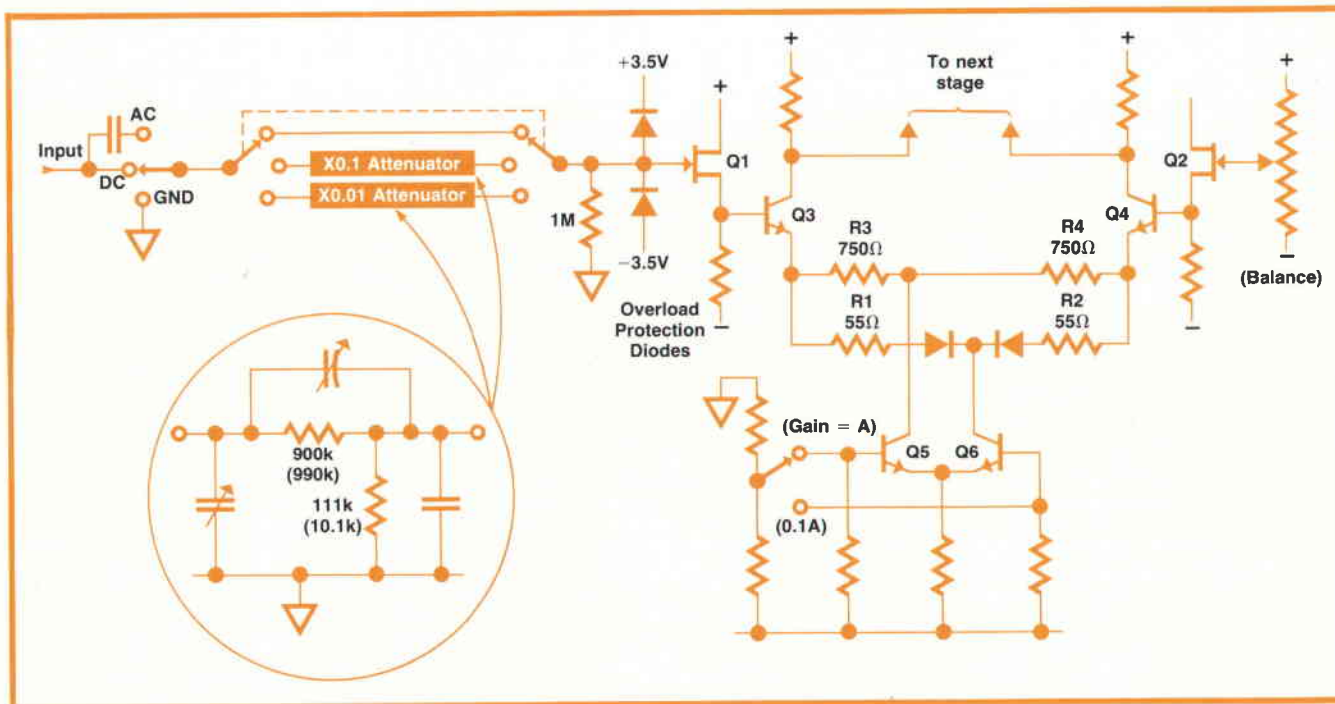


Fig. 7. Vertical input needs only two frequency-compensated attenuator sections. The other ranges are obtained by using dc voltages to switch the gain of the amplifiers.

Q11. A constant-current source supplies more current for charging the distributed load capacitance than a passive load would (at the same power dissipation), thus speeding up the transient response.⁴ However, the steady-state current flow normally establishes the maximum charge rate. To permit the steady-state current to be small, and hence keep power dissipation low, the current source in this circuit is modulated by the signal through capacitor C11. High-speed transients passing through C11 to Q13 increase available current during fast transients to speed up the response of the amplifier. This configuration thus gives fast transient response with low steady-state current.

The circuit shown in Fig. 8 supplies the drive voltage for one CRT vertical deflection electrode and an identical amplifier drives the other electrode in the opposite phase. The horizontal drive amplifiers use a similar configuration but with higher-voltage transistors operating from a +210V supply. This obtains the higher drive voltage needed for the horizontal deflection plates.

Logical Triggering

Triggering is often a problem with oscilloscopes, most of the problems arising because a new trigger may occur before the sweep circuits have fully recovered from the previous sweep. This results in an erratic display.

Basically, the new oscilloscopes' trigger and

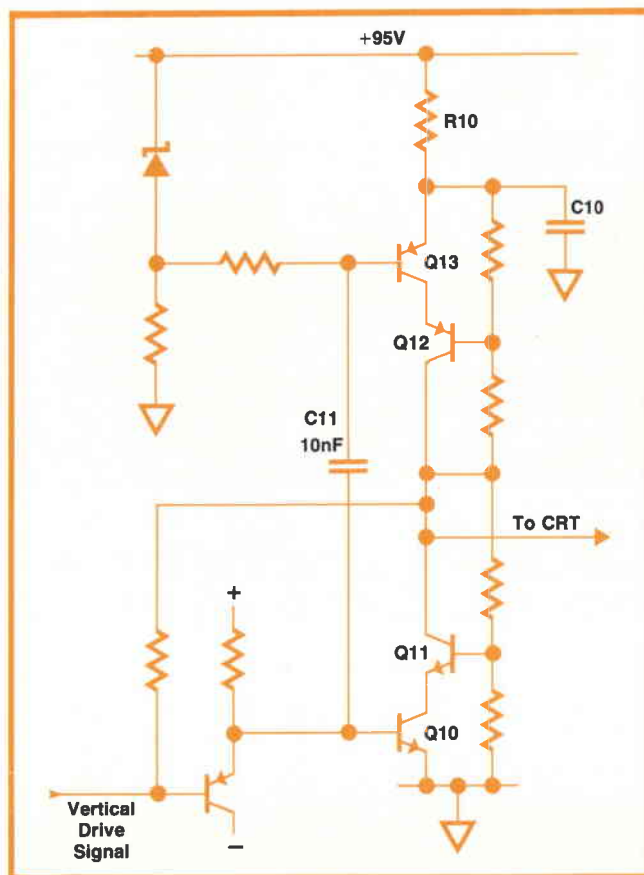


Fig. 8. Output stage uses a cascode driver (Q10, Q11) with a constant-current load (Q12, Q13). R10 establishes the steady-state current.

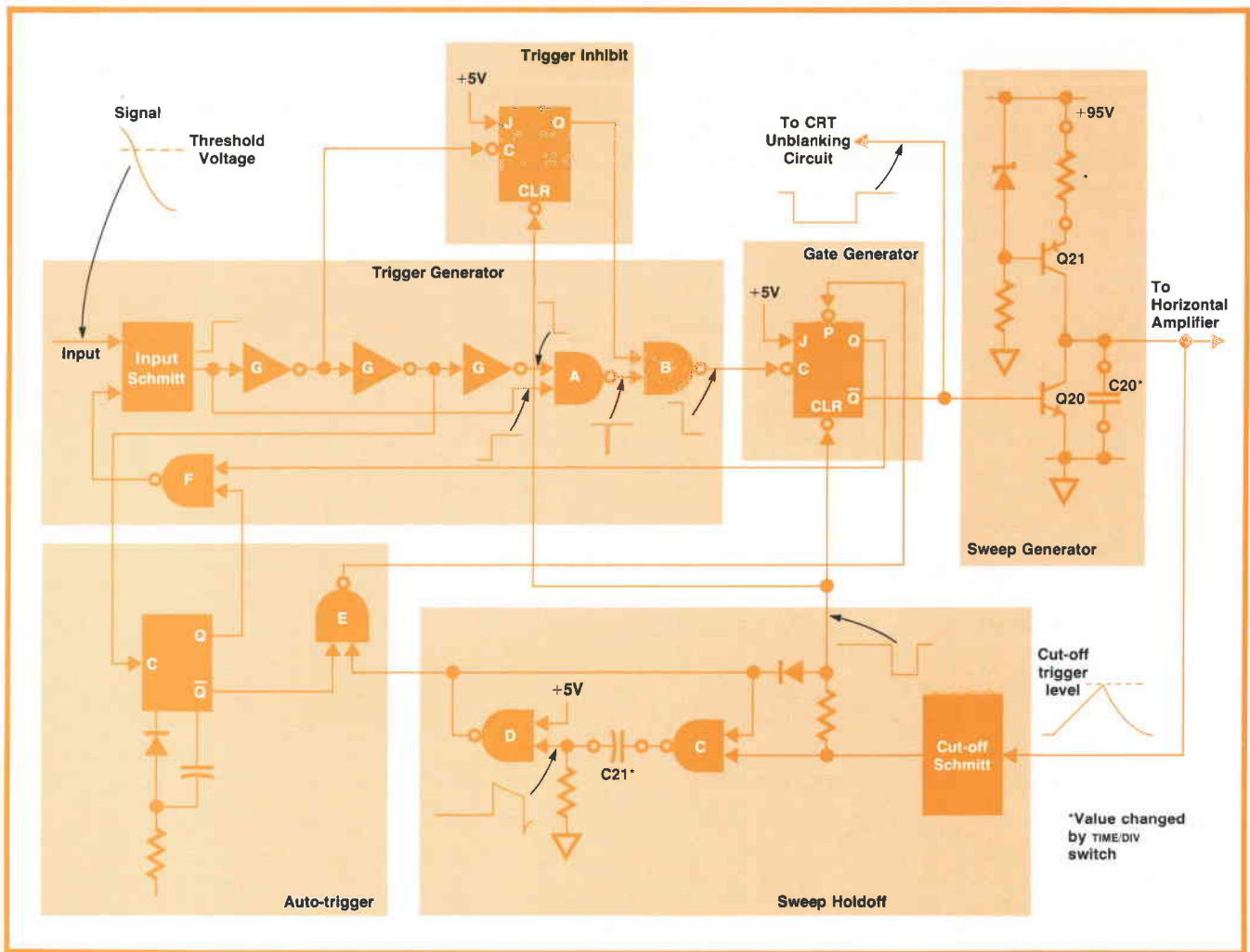


Fig. 9. Trigger and sweep generating circuit uses two holdoffs to prevent erratic sweeps (see text).

sweep circuits follow established laboratory oscilloscope practice. The trigger signal is applied to a differential amplifier and the polarity switch selects one of the inputs according to the trigger slope desired (Fig. 4). The negative-going slope of the output switches a Schmitt trigger as it crosses the threshold-voltage level (Fig. 9). The resulting positive-going step at the output of the Schmitt circuit triggers the gate generator, a flip-flop. It in turn switches off the ramp capacitor discharge switch (Q20 in Fig. 9) and unblanks the CRT. Ramp capacitor C20 now charges through constant-current source Q21, generating the sweep voltage. Once triggered, the Q output of the gate generator holds off the Schmitt trigger by way of gate-inverter F.

When the sweep ramp reaches 10V, it triggers the cutoff Schmitt trigger circuit which in turn resets the gate generator flip-flop. To prevent retriggering while the ramp capacitor is discharging, the negative-going reset trigger is processed through NAND gates

C and D, which act as a sweep hold-off circuit. The output of gate D, which serves merely as an inverter, is fed back to gate C, clamping the output of gate D low until sweep holdoff capacitor C21 discharges sufficiently to allow the gate D output to rise again. By holding the CLR input to the gate generator low while sweep holdoff capacitor C21 discharges, gate D prevents a new sweep from being initiated during the holdoff period.

This raises a new problem—an erratic sweep could occur if a trigger arrives at the gate generator at the same time that the holdoff circuit is removing the CLR signal. An erratic sweep would result because the switching time of the gate generator would be different in this case. Therefore, a trigger inhibit flip-flop and a signal delay have been added.

Normally, the low-to-high transition at the output of the input Schmitt trigger initially causes a high-to-low transition at the output of gate A, but the Schmitt transition is also delayed and inverted in in-

verters G so it causes the gate A output to go high again a few nanoseconds later. This delayed transition passes through gate B and triggers the gate generator, starting the sweep. Gate B was enabled by the trigger inhibit circuit which had been clocked by the Schmitt trigger a few nanoseconds earlier.

During the holdoff period, the triggering transition cannot pass gate B so long as the trigger inhibit flip-flop's Q output is held low by the holdoff signal at the CLR input. However, if a trigger arrives at the trigger inhibit flip-flop at the same time that the holdoff signal is being removed, the switching time of the Q output would be affected, but this causes no problem because the transition will be complete by the time the trigger arrives at gate B because of the delays in the inverters G. Thus it is not possible for a trigger to arrive at the gate generator at the same time the holdoff signal is being removed. The result is solidly stable triggering.

The total delay from trigger Schmitt transition to CRT unblanking and sweep start is about $0.1\mu\text{s}$.

Always a Baseline

In the absence of triggers, the sweep circuit becomes self-triggering so the CRT trace is never lost—there is always a baseline. The trailing edge of the holdoff pulse starts a new sweep whenever the autotrigger circuit enables gate E.

The autotrigger circuit is a monostable multivibrator. With no input triggers, the Q output of this circuit is high, allowing the output of gate E to go low on occurrence of the trailing edge of the sweep reset pulse. The negative-going step out of gate E is applied to the "preset" input of the gate generator, starting a sweep. As long as gate E is enabled, sweeps will occur automatically.

An input trigger sets the autotrigger monostable multivibrator, blocking gate E. The monostable resets itself 0.5 s after the last input trigger so in the absence of any input triggers, a baseline appears on the CRT. Whenever there are triggers, the monostable remains in the set state and gate E is closed, preventing self-triggering of the sweeps.

Few Parts

The two Schmitt triggers are on one integrated circuit and the two flip-flops on another. Four of the gates are on one IC and two more are on another (two other gates in this IC are used elsewhere in the instrument). All three amplifiers in the delay chain are on one IC (three other amplifiers in the same IC are used elsewhere). In other words, most of the trigger circuitry is implemented with six integrated circuits, and these are low-cost, standard TTL logic circuits, another example of how improved performance can now be obtained at lower cost.

TV Sync

Because it is expected that these oscilloscopes will find wide use in service shops, a TV sync separator is included (Fig. 4). This works along conventional lines in that it clamps to the peak value of a composite TV waveform and clips off 60% of the waveform, leaving the TV sync pulses. These are cleaned up by applying them to a Schmitt trigger before sending them on to the sweep trigger circuit, or they are passed through a low-pass filter to obtain the vertical sync pulse, then shaped by a Schmitt trigger. The vertical pulses are passed to a $\div 2$ circuit, however, so that the resulting triggers occur on every second field, and hence at the same point in each frame for a clean display.

Economical Regulated High-Voltage

To assure a constant deflection factor and hence deflection accuracy, the new oscilloscopes have a regulator on the high-voltage supply for the accelerating electrodes. Recent practice has been to derive the accelerating voltages by using an ultrasonic oscillator to drive a step-up transformer that supplies the high-voltage rectifier, making it possible to apply level control signals at low voltage levels to the oscillator.

The Models 1220A and 1221A have a high-voltage regulating system that does not require a separate os-

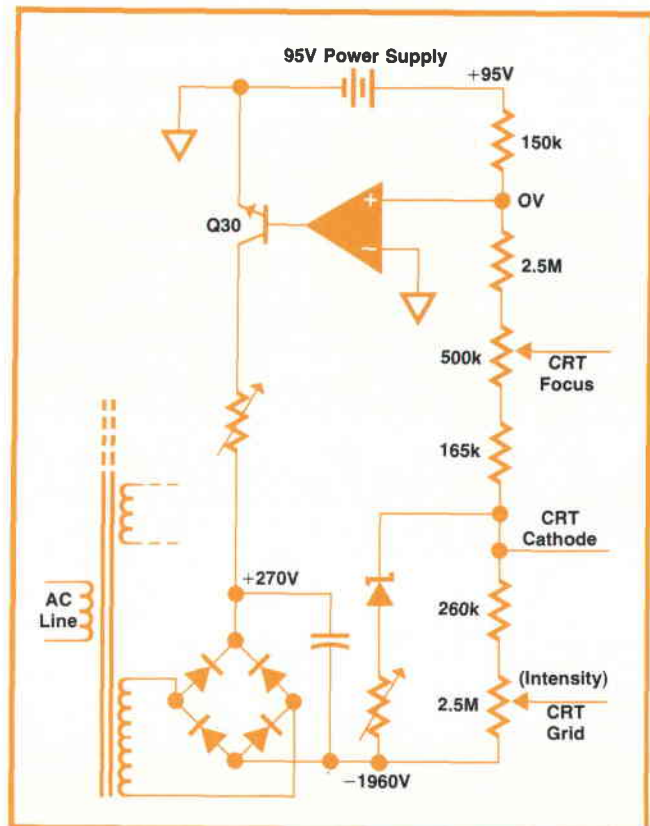


Fig. 10. High-voltage power supply uses a regulator that operates at low voltage levels.

cillator to enable control with low voltages. As shown in the diagram of Fig. 10, the high voltage is obtained from a separate winding on the power transformer. The ground return, however, passes through a series-pass transistor Q30. The regulator amplifier causes the voltage drop across Q30 to change in the right amount to compensate for voltage changes in the high-voltage supply, as sensed at a tap on the resistive divider, using the regulated 95V supply as a reference.

All the other voltages in the oscilloscope are regulated too, a feature that costs relatively little to implement nowadays because of the availability of low-cost integrated-circuit regulators.

Acknowledgments

The Models 1220A and 1221A Oscilloscopes resulted from the efforts of many people. Project leader was Ulrich Hubner, who also designed the high-voltage power supply and blanking circuits.

Stefan Traub developed the vertical amplifiers while Frank Rochlitzer and Horst Schweikardt designed the sweep and trigger circuits. Mechanical design was by Rudiger Plessner and Bruno Holzer with the assistance of Siegfried Dippon of the process engineering group.

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SPECIFICATIONS

Models 1220A and 1221A Oscilloscopes

Modes of Operation (1220A)

CHANNEL A; CHANNEL B: channels A and B displayed alternately on successive sweeps (Alt), triggering by A channel; channels A and B displayed by switching between channels at approx 200 kHz rate with blanking during switching (Chop); automatic selection of alternate or chop mode. Chop, at sweep speeds from 0.5 s/cm to 1 ms/cm; Alt, 0.5 ms/cm to 0.1 μ s/cm

Vertical Amplifiers

BANDWIDTH: (3 dB down from 50 kHz, 6 div reference signal from a terminated 50-ohm source)
DC-COUPLED: dc to 15 MHz
AC-COUPLED: lower limit is approx 2 Hz
RISETIME: approx 23 ns

DEFLECTION FACTOR

RANGES: from 2 mV/cm to 10 V/cm in 1, 2, 5 sequence $\pm 3\%$ accuracy with vernier in calibrated position on 10mV/cm to 10V/cm ranges. $\pm 5\%$ on 2 and 5 mV/cm ranges
VERNIER: continuously variable between ranges, extends maximum deflection factor to 25 V/cm

INPUT RC: approx 1 M Ω shunted by approx 30 pF

INPUT COUPLING: ac, dc, or gnd selectable. Gnd position disconnects signal input and grounds amplifier input.

Time Base

SWEEP

RANGES: from 0.1 μ s/cm to 0.5 s/cm in 1, 2, 5 sequence $\pm 4\%$ accuracy with Expander in calibrated position
EXPANDER: continuously expands sweep to more than 10 times. Maximum usable sweep speed is approx 20 ns/cm

SWEEP MODE: sweep is triggered by internal or external signal. Bright baseline displayed in absence of input signal.

TRIGGERING

INTERNAL: approx 2 Hz to 15 MHz on signals causing 1 cm or more vertical deflection.

EXTERNAL: approx 2 Hz to 15 MHz on signals 0.1 V p-p or more
EXTERNAL INPUT RC: approx 1 megohm shunted by approx 30 pF
LINE TRIGGERS: on line frequency
TV SYNC: separator for + or - video, requires 1 cm of video signal to trigger; automatic frame (0.5 s/cm to 100 μ s/cm) and line select (50 μ s/cm to 0.1 μ s/cm). Usable also as a low-pass filter.

LEVEL AND SLOPE

INTERNAL: at any point on positive or negative slope of displayed waveform
EXTERNAL: continuously variable from +0.5V to -0.5V on either slope of trigger waveform. -10 extends trigger range to +5V to -5V.

External Horizontal Input

BANDWIDTH: dc to 1 MHz
COUPLING: dc

Expander	Input Attenuator	Deflection Factor
Cal	1:1	1V/cm
Cal	1:10	10V/cm
cw	1:1	100mV/cm

Continuous adjustment between ranges by Expander
INPUT RC: approx 1 megohm shunted by approx 30 pF
X-Y PHASE SHIFT: -3° at 100 kHz

Cathode-Ray Tube and Controls

TYPE: mono-accelerator, approx 2 kV accelerating potential, P31 phosphor
 Blue light filter furnished. P7 phosphor and amber filter in lieu of P31 available
GRATICULE: 8 \times 10 cm internal graticule, 0.2 cm subdivisions on major horizontal and vertical axes

BEAM FINDER: returns trace to CRT screen regardless of setting of horizontal and vertical controls.

PROBE ADJUST: approx 3 V peak, 2 kHz square wave for adjusting probe compensation.

INTENSITY MODULATION: ± 5 V (TTL compatible) dc to 1 MHz blanks trace of any intensity. Input R approx 1 k ohm.

General

POWER: 100, 120, 220 V, $\pm 5\%$, -10% 48 to 66 Hz, approx 35 W

WEIGHT:

1220A: net, 16 1/4 lb (7.3 kg)
 1221A: net, 15 1/2 lb (7.0 kg)

DIMENSIONS: 12 1/2 in W \times 7 1/4 in H \times 16 1/4 in D (31.1 \times 18.1 \times 41.3 cm)

OPERATING ENVIRONMENT

TEMPERATURE: 0 to +45 $^\circ$ C; non-operating to 75 $^\circ$ C

HUMIDITY: to 95% relative humidity to +40 $^\circ$ C

ALTITUDE: to 15,000 ft (4600 m)

VIBRATION: vibrated in three planes for 15 minutes each with 0.010 in (0.25 mm) excursion, 10 to 55 Hz.

Accessories

VOLTAGE DIVIDER PROBE: Model 10013A 10-to-1 voltage divider probe provides 10 M Ω input resistance shunted by 10 pF. Maintains full 15 MHz bandwidth.
CAMERA ADAPTER: Model 10373A Camera Adapter allows Model 123A Camera to be used.

FRONT PANEL COVER: Model 10117A Front Panel Cover provides protection and storage space for probes.

RACK MOUNTING KIT: Model 10119A Rack Mounting Kit mounts 1220A or 1221A oscilloscopes in standard 19 in (48.3 cm) rack requiring only 8 1/4 in (22.2 cm) of vertical space.

PRICES IN U.S.A.

Model 1220A Dual Channel Oscilloscope, \$695

Model 1221A Single Channel Oscilloscope, \$575

P7 phosphor instead of P31, add \$20

Model 10013A Voltage Divider Probe, \$30

Model 10373A Camera Adapter, \$45 (tentative)

Model 10117A Front-panel Cover, \$20

Model 10119A Rack Mounting Kit, \$65

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Hans-Günter Hohmann

Obtaining a Diplom Ingenieur in electronics from the Technische Hochschule in Aachen, Germany, in 1967, Hans-Günter Hohmann joined Hewlett-Packard GmbH shortly thereafter, starting in research and development on instruments for acoustic measurements. He subsequently became project leader on several products, including the 8064A Real-Time Audio Spectrum Analyzer, and group leader for acoustic products. He then became group leader for low-cost oscilloscopes. Active in seasonal sports and other light athletic events, Hans-Günter also enjoys reading about history, both natural and cultural. Since becoming a father a year ago he does less of the former and more of the latter.

Laboratory Notebook

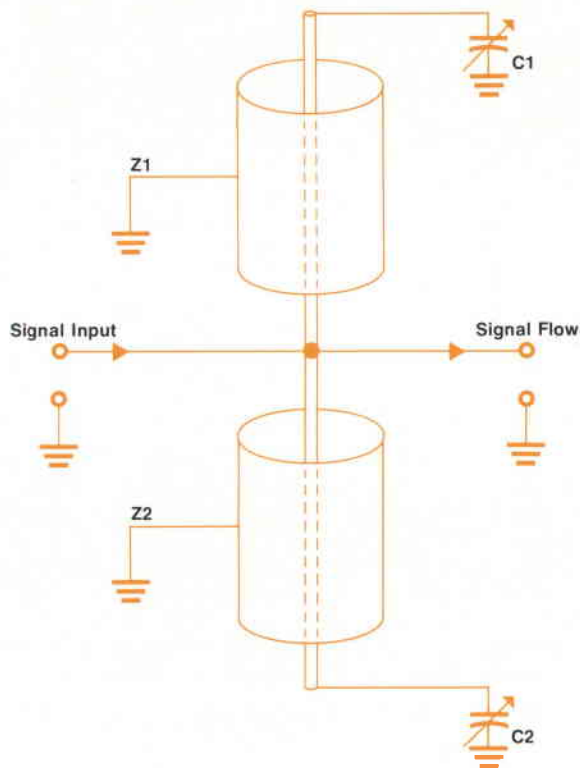
Sharp Cut-off Filters for That Awkward UHF Band

With discrete components too lossy, and cavities too bulky, the design of compact, sharp cut-off filters for the frequencies between 200 and 1000 MHz poses a problem.

In designing the Model 78101A ECG Telemetry Receiver,* we faced this problem. Here was needed a filter that would remove an image frequency at 423 MHz without overly attenuating the carrier at 467 MHz (IF of 22 MHz and LO at 445 MHz). Ordinarily this would be done with bandpass filters, several in series being required to get adequate rejection in this frequency band. Several filters in series, though, means considerable loss.

This problem was solved by using a transmission-line filter. This filter is not only effective, but it is also inexpensive.

Shown in the drawing below, the filter has two transmission-line sections that form a series-resonant trap for the image frequency and a parallel-resonant passband for the carrier. Operation is as follows: Capacitor C1 tunes transmission-line Z1 to series resonance at 423 MHz, thus effectively shorting out any



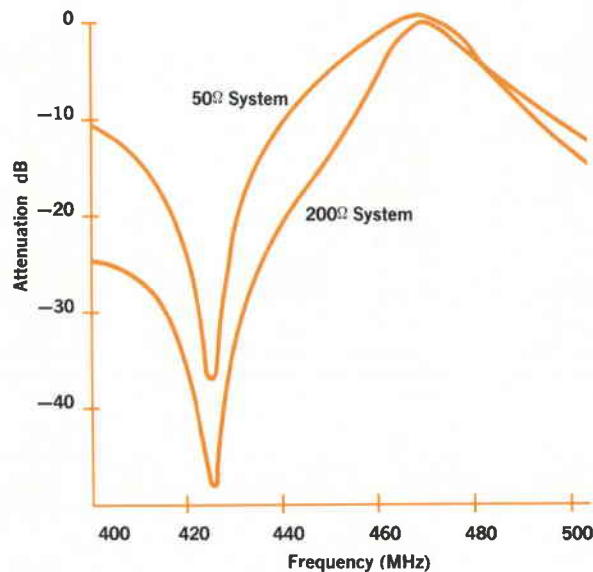
signals at the image frequency. At higher frequencies, Z1 is inductive but transmission-line Z2, being shorter, is capacitive. C2 is tuned to resonate Z2 with Z1 at 467 MHz so the carrier 'sees' a parallel resonant circuit, and passes with negligible loss.

As shown in the plot of frequency response, this design easily achieves more than 35 dB rejection of signals at the image frequency in a 50Ω system, and more than 45 dB in a 200Ω system.

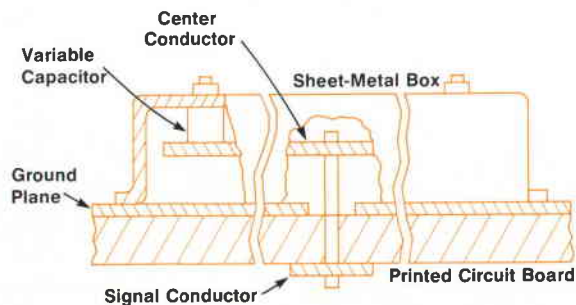
Design Execution

There are a number of ways that such a circuit can be constructed. Using lengths of coaxial cable was not entirely satisfactory, however, because the fringing fields at the open ends of the cable where the capacitors are attached interacted with other filters nearby.

*Larsen et al., "An Effective ECG Telemetry System," Hewlett-Packard Journal, April 1972.



The design that evolved uses a long, narrow, sheet-metal box with an open side that is clamped to the ground plane of a printed-circuit board, forming the outer conductor of a coaxial line. The center conductor is a flat bar mounted at each end by a trimmer capacitor, as shown in the drawing. This forms a completely shielded, low-loss, air-dielectric transmission line.



The single structure contains both sections of coaxial line. The signal lead, brought from the other side of the printed-circuit board through a hole in the ground plane, attaches to the center conductor at the point that divides the line into the series-resonant and parallel-resonant sections. Actually, two signal leads are used, one for the input to the filter and one for the output, eliminating a common impedance between input and output that would degrade performance. These leads attach on opposite sides of the center-conductor bar.

Two of these filters are used in the HP Model 78101A ECG Telemetry Receiver, one at the antenna input and one at the output of the two-stage tuned RF amplifier. Overall, an image frequency rejection of more than 100 dB is obtained.

James Larsen
Richard Dilman
Richard Tverdoch

Medical Electronics Division

A Data Error Analyzer for Tracking Down Problems in Data Communications

A combined data generator and self-synchronizing receiver, this new instrument makes six different measurements simultaneously, helping to pinpoint sources of trouble in data communications systems.

by Jeffrey R. Duerr

WITH THE GROWING USE of voice-communication channels for the transmission of digital data, maintaining transmission reliability becomes of increasing concern.

Reliability can be enhanced by repeating messages or by transmitting at slower rates, which means less efficient use of facilities, or it can be enhanced by the use of error-correcting codes, which implies more complex equipment. On the other hand, increased reliability results from consistently maintaining optimum system performance.

Making sure that optimum performance is maintained at all times has not been as simple and straightforward as one might surmise. The transmission of digital data over any distance often involves sophisticated equipment designed and manufactured by several different firms. The data may originate in a keyboard/display terminal or a computer made by one firm, be coupled to someone else's telephone system by a modem made by still another firm, be transmitted over the telephone system to another modem, and finally reach the receiving terminal or computer. The system is usually a combination of the efforts of a terminal manufacturer, a separate modem manufac-

turer, a representative of the telephone company, and an in-house technician, none of whom are liable to be involved in a comprehensive view of the whole system.

Diagnostic programs that can show whether or not a system is operating satisfactorily have been written, but interpreting results when the system does not operate properly is often hard to do, especially since those who understand the diagnostics may not have a good understanding of the various parts of the system.

For these reasons a new instrument was conceived, an instrument sufficiently complex to fully exercise a sophisticated data link yet simple enough to be operated without detailed knowledge of the various parts of the system under test. Information presented by the instrument is unambiguous and easily interpreted to help track down the system component at fault.

This instrument, Model 1645A Data Error Analyzer (Fig. 1), is designed primarily to survey data communications systems that use voice-grade phone lines. It derives the information necessary to approach solutions to network problems by generating

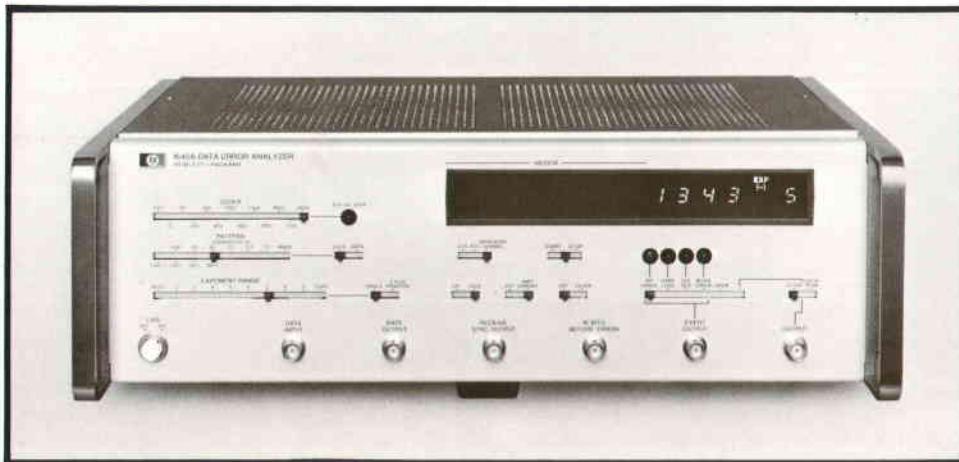


Fig. 1. Model 1645A Data Error Analyzer generates digital test patterns in its transmitter section, transmits the patterns through a communications channel, and analyzes the received patterns in its receiver section by comparing them to locally-generated patterns. It analyzes the patterns six ways simultaneously.

and interpreting digital patterns. It operates at 12 standard bit rates from 75 to 9600 bits/s but it can analyze synchronous systems* at any bit rate up to 5 Mbits/s.

Multiple Tests

The Analyzer generates pseudorandom bit sequences for the data input. At the receiving end, it compares the received sequence to a locally generated sequence identical to the transmitted sequence. For end-to-end measurements, two instruments are used, but because the instrument contains both transmitting and receiving circuits, only one is needed for loop-around tests.

The instrument makes several tests as it compares the received and locally generated sequences. Besides measuring bit-error rate, which gives a measure of how well a digital transmission system is performing, it measures several other parameters to help localize problems. The tests it performs are:

- **Bit error rate (BER)**, the ratio of number of incorrect bits to number of bits received. It is fast becoming the preferred indicator of digital transmission quality.
- **Block error rate (BKER)**, the ratio of the number of data blocks that have errors to the number of blocks received. In the 1645A, each block has 1000 bits. When compared to bit-error rate, this indicates the distribution of error, that is, whether they are evenly distributed or whether they occur in bursts.
- **Skew**, a comparison of the number of times that a "1" data bit is in error to the number of times that a "0" is in error. As measured by the new Data Error Analyzer, skew is the percentage of time that "1's" are in error with respect to total errors. If the reading is not consistently near 50%, it indicates that the errors may be pattern sensitive or that a decision threshold somewhere in the system is improperly set.
- **Jitter**, which is peak-to-peak timing variations in the received bits expressed as percent of nominal bit period. This can be the result of power line pickup or other interference with the timing of the system.
- **Total peak distortion**, which is jitter plus bias, bias being a condition where marks, or "1" data bits, are consistently of a different length from the spaces, or "0" data bits, expressed as a percent of nominal bit period. It usually results from an improperly set threshold level and often results in skew.
- **Clock slip**, the number of times that data jumped one bit period or more during the selected measurement interval. It usually results from phase hits caused by path switching in the transmission link or it could be caused by slippage of the bit synchronizer in a synchronous modem.

* A synchronous system is defined as one where system timing is synchronized to a master clock in the transmitting modem. A clock-recovery circuit in the receiving modem reconstitutes the master clock for the terminal. In an asynchronous system, timing is controlled by the terminal, e.g., a teletypewriter.

- **Carrier loss**, expressed as the number of times that input data faded during the measurement period. An output is provided so the number of bits lost can be totaled by an external counter to derive a measure of total lost time.

Organizing Test Results

Errors are accumulated for a time interval equivalent to the number of bits selected by a front-panel switch, which gives a choice of 10^2 to 10^9 bits in decade steps. Tests may also be conducted in an AUTO mode that terminates a test on the next decade number of bits received after 98 errors have been counted. This assures valid (non-overranged) readings when the instrument must be left unattended. Tests may also be started and stopped manually.

Single tests can be made, each in response to a front-panel switch, or tests may be repeated automatically.

Regardless of the test selected for display during the measurement interval, front-panel indicators flash to show occurrence of each of four types of errors (BER, BKER, clock slip, carrier loss). During the test, the display presents a continuously updated indication of number of errors. Results of all tests are stored internally and at the conclusion of the measurement interval, are made available for readout individually, as selected by a front-panel switch. This permits comparison of all values obtained on the same data, an aid in diagnosing problems. The results of any four tests are also printed sequentially if an external printer is used, permitting long-term, repetitive tests to be conducted unattended.

The instrument outputs a pulse once per received digital sequence, enabling oscilloscope viewing of the received sequence. It also outputs a pulse whenever an error is detected. One of the uses for this output is to trigger an oscilloscope or logic analyzer when an error occurs, so the 16 bits that precede the error can be displayed. A 16-bit delay makes the last 16 bits available at a front-panel connector. This is useful in determining whether certain bit patterns cause the errors.

The time lapse between a data edge and an internal clock reference is available at a front-panel connector as an analog signal. This allows oscilloscope study of the cyclic nature of any jitter, often helping by providing clues as to the cause of the jitter, e.g., powerline pickup.

Where It Goes

In evaluating a system, the Data Error Analyzer usually connects to the modem in place of the terminal. Accordingly, it generates and responds to the "handshake" signals used by modems. The display includes the necessary indicators (DATA SET READY,

CLEAR TO SEND) and a front-panel switch selects the control status (DATA TERMINAL READY, REQUEST TO SEND). The switch also has a BACKWARD CHANNEL position to allow tests involving the modem's supervisory channel.

Interface is by way of a plug-in circuit card and connector (Fig. 2) that can be changed to meet the requirements of different interface standards. Normally, the instrument is supplied with a card that meets the logic-level and pin numbering requirements of EIA specification RS232C (CCITT V 24).

TTL-compatible inputs and outputs through BNC connectors on the front and rear panels facilitate use of the instrument in the lab and in other special situations.

Test Patterns

A front-panel switch selects one of seven digital sequences in NRZ (non-return to zero) format for transmission and at the same time it sets the receiver circuits to the identical pattern. Four pseudorandom bit sequences (PRBS) are available (63, 511, 1047, and 1 048 575 bits) and there are three mark:space pat-

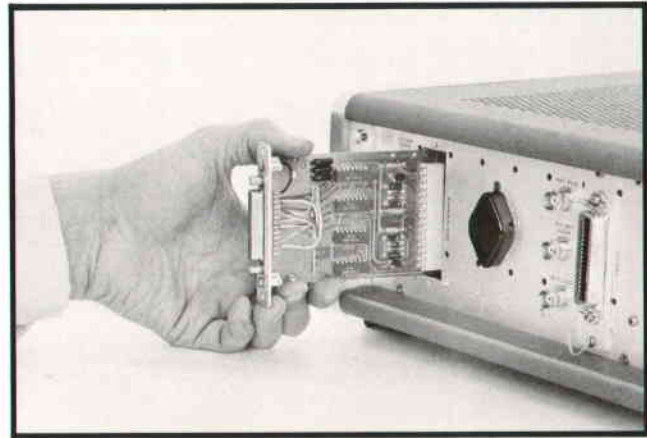


Fig. 2. Plug-in modules interface the Data Error Analyzer to the system to be tested. The circuit card converts the instrument's logic levels to those required by the system. An appropriate connector is included.

terns, a single mark (or "1") preceded by 1, 3, or 7 spaces ("0"), a greater range of test sequences than CCITT requirements. A DATA/DATA switch allows the complement of the selected pattern to be used, e.g., a

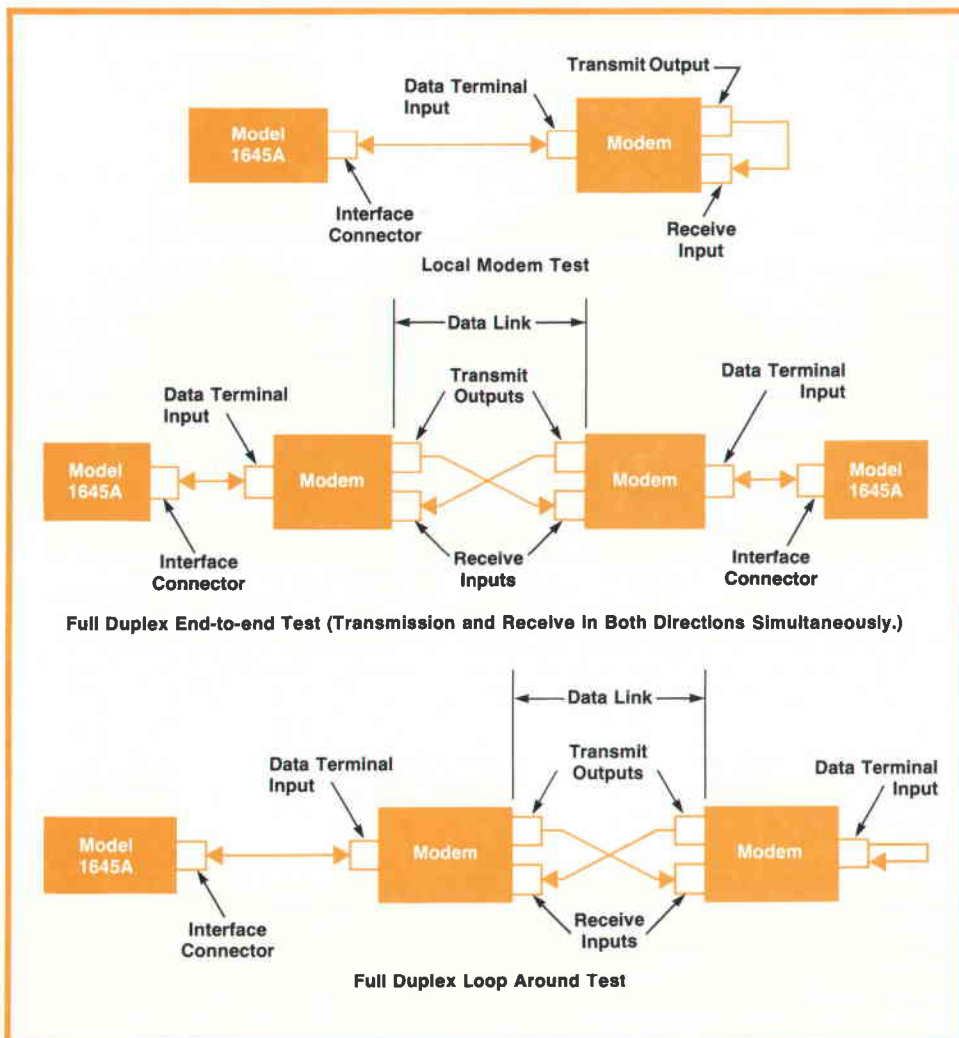


Fig. 3. Some of the ways by which the Data Error Analyzer is connected to a system for tests.

single space preceded by seven marks.

The pattern selector switch also has a MARK position that simply places a dc level on the output.

In end-to-end measurements, as long as the receiving instrument is set to the same pattern and bit rate as the transmitting instrument, the receiver circuits automatically synchronize to the transmitted bit rate and automatically align the locally-generated bit sequence to that transmitted. The receiving circuits also sense whether or not the polarity of the transmitted bit sequence may have been inverted during transmission and perform a re-inversion if necessary. Furthermore, the display circuits are autoranging. Thus, in routine tests the operator need concern himself only with setting the pattern and bit-rate switches and selecting the time duration of the test.

The instrument also has a LOOP mode that internally couples the transmitting circuits directly to the receiving circuits to verify that the instrument is operating correctly. One bit in each PRBS sequence can be made a deliberate error so the operation of the error-detecting circuits can be confirmed.

Some of the ways that the Data Error Analyzer may be connected to a system for tests is shown in Fig. 3. The manner in which it used to track down a problem is shown by the troubleshooting diagram of Fig. 4.

Instrument Operation

A block diagram of the Data Error Analyzer is shown in Fig. 5. The pseudorandom digital sequences are generated in a shift register that has feedback through exclusive-OR gates to its input from selected stages within the register. The mark:space sequences are generated by a counter that resets after a selected number of counts.

The clock frequency is divided down from a 5.76 MHz crystal oscillator to one of the standard modem clock frequencies, or it can be supplied by an external source.

The selected sequence is supplied to the front panel through a TTL-level buffer and to the interface module that converts the sequence to levels suitable for the system to be tested. These are the only circuits concerned with the transmit function. All the others belong to the receiver.

The test sequence, after transmission through the unit or system under test, is brought into the instrument either through a front-panel connector (not shown) or through the interface module. It is then distributed to the various circuits.

Receiver timing is controlled by the bit synchronizer. This has a stable 5.76 MHz oscillator that is phase-locked to the incoming data stream. The output of the oscillator is divided down to derive the selected clock frequency. It is not used, however, if an external clock is supplied.

Checking for Errors

The incoming data is compared bit by bit to the output of a closed-loop shift register that is configured the same as the transmitting shift register. Whenever the two bit sequences differ, an error is counted.

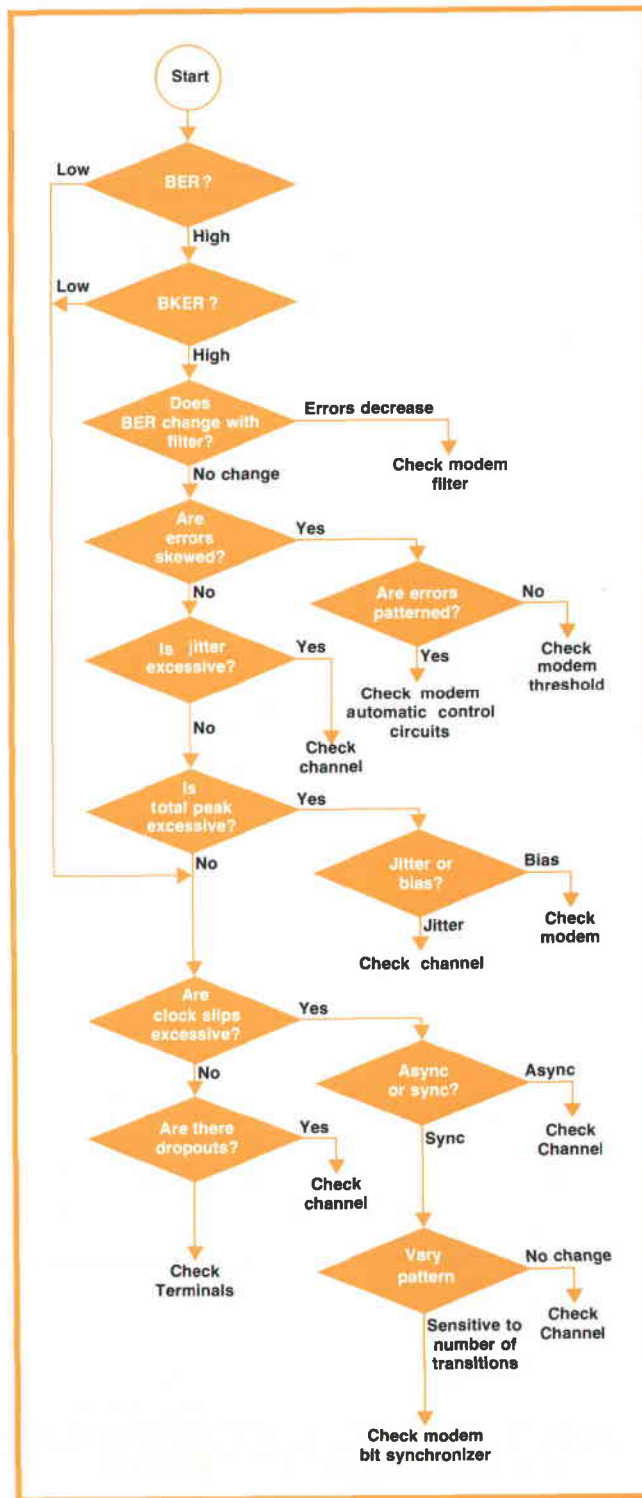


Fig. 4. Troubleshooting diagram shows how various test results are used to track down problems in a data communications system.

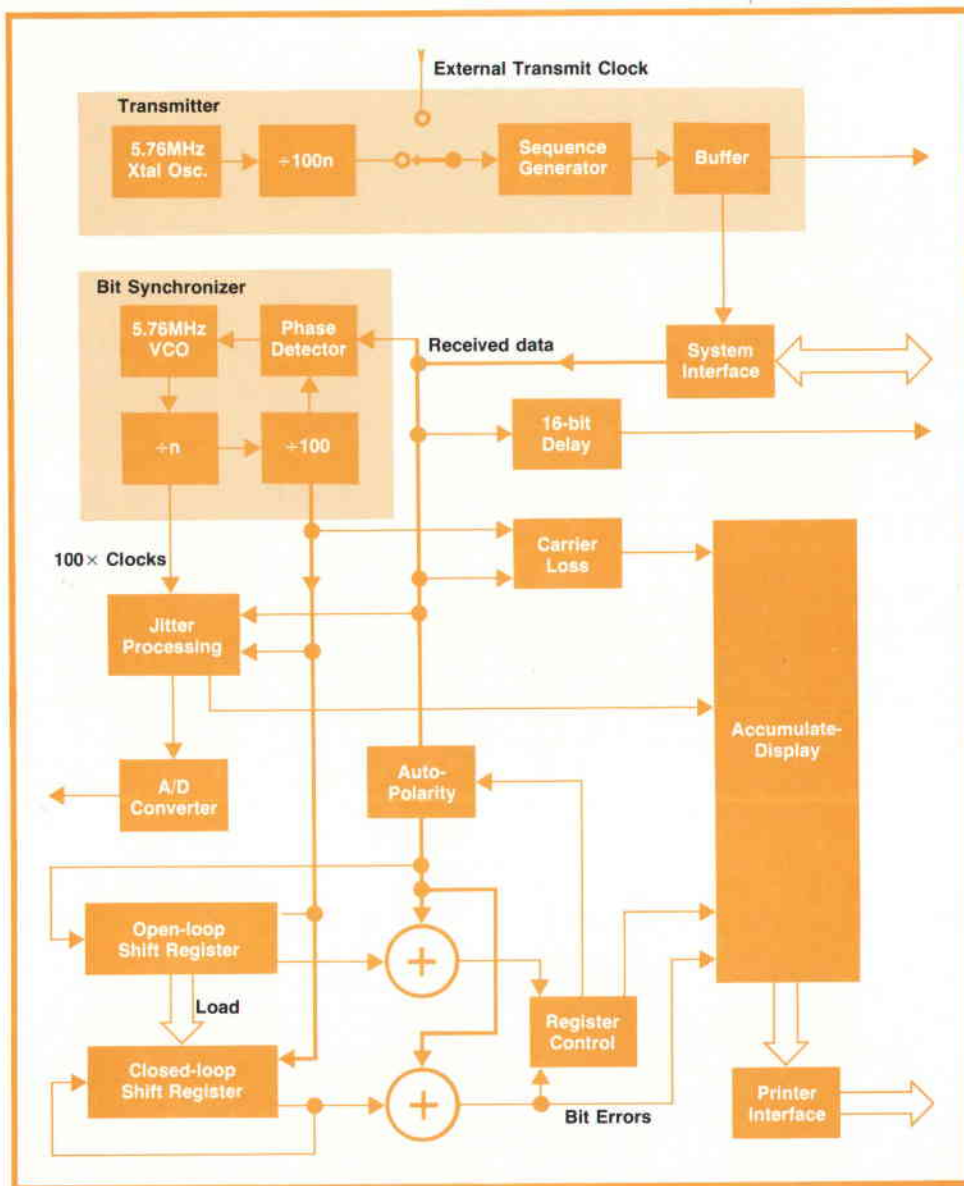


Fig. 5. Block diagram of Model 1645A Data Error Analyzer.

From this, measurements of bit-error rate are derived.

The incoming data is also compared to the output of an open-loop shift register that uses the same exclusive-OR gate configuration as the transmit register but which has no feedback connection. This register is used for synchronizing the closed-loop shift register, for detecting clock slip, and for detecting the need for inverting the polarity of the incoming data stream, as will be described subsequently.

Block-error rate is measured by incrementing a counter every 1000 bits only if one or more errors had occurred during the 1000-bit block. Skew is measured by totaling all errors in one counter and only the 1's errors in a second counter. When the all-error counter overflows on a count of 100 (actually 98 because of internal logic), the contents of the 1's-only counter is latched out as the measure of skew.

The jitter/bias circuit compares the timing of the data edges to clock pulses derived from the phase-locked oscillator. From this comparison, values for jitter and total peak distortion are derived.

Carrier loss is detected by a counter that totals clock pulses between data transitions in the incoming data stream. If more than 16 clock periods elapse without a data transition, it is assumed that a dropout occurred. For the long pseudorandom sequence, which has up to 20 bits without a transition, the decision threshold is set to 32. The error measuring circuits are inhibited when carrier loss is detected so as not to count false errors beyond those counted during the detection period. The error count resumes, however, after the carrier returns so measurements are not aborted by a carrier loss.

The incoming data is also applied to a 16-bit shift register that serves for temporary storage. This

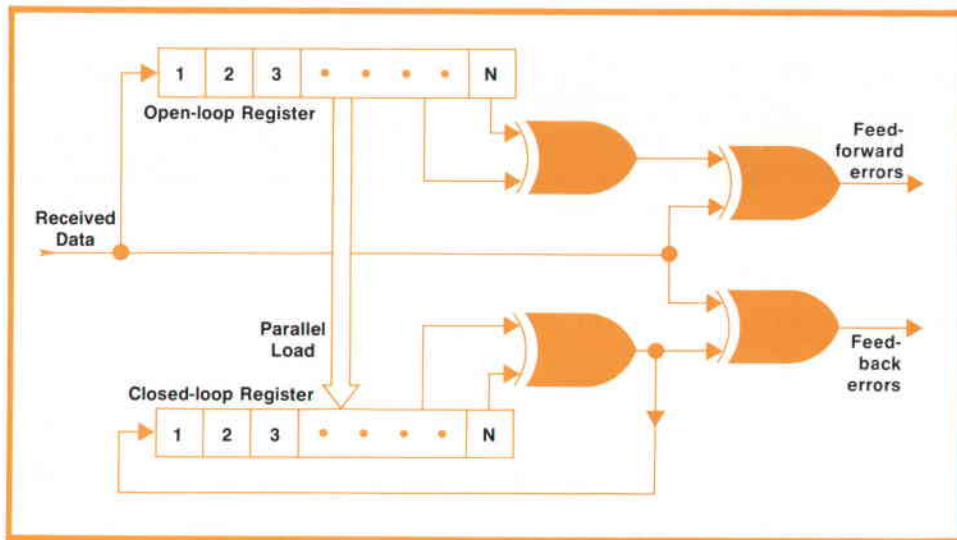


Fig. 6. Simplified diagram illustrates concept behind closed-loop (feedback) and open-loop (feedforward) registers and how the two configurations are used in the Data Error Analyzer.

makes the 16 bits that precede an error available for examination.

Automatic Sync

For the error detection circuits to work, the closed-loop shift register in the receiver must operate in synchronism with the shift register in the transmitter. Frame sync, as it is called, is accomplished with the help of the open-loop shift register.

By way of explanation, the two shift register configurations are shown in Fig. 6. The output of the closed-loop or feedback register is passed through an exclusive-OR gate and fed back into the input. There is an output from the exclusive-OR gate only when its inputs differ, so the output of the feedback register may or may not be fed back unaltered depending on the state of the other input to the gate. With proper choice of feedback taps (and precautions to assure that the shift register is never in the all-zero state), the shift register generates all possible combinations of N ones and zeros, except all zeros, where N is the number of states in the register.

If the same PRBS sequence generated by the feedback register were fed into the open-loop or feedforward register, the output of the feedforward register would be identical to its input, just as though it were supplying its own input. If, however, an error were injected into the input stream, it would cause two errors at the output (once in each stage connected to the exclusive-OR gate). Open-loop shift registers therefore are not accurate indicators of bit-error rate, not only adding errors but also cancelling errors when there is more than one error in the register. However, frame sync with the data stream is automatically achieved as soon as the data loads N bits into the register.

These properties are used to advantage in the new Data Error Analyzer. As shown in Fig. 6, the incom-

ing bit stream is fed only to the feedforward register but it is compared to the outputs of both registers. The instrument, however, counts only the errors from the feedback register when measuring bit-error rate.

The comparison of the errors detected by the two registers determines the course of action within the instrument. At startup or following a clock slip, both registers will be out of frame sync, but within N bits the feedforward register will be loaded by the incoming data and will stop generating errors. The feedback register, on the other hand, continues to generate errors.

Errors from the feedback register are totaled in a counter that is reset by errors from the feedforward register. If the counter overflows, indicating a great excess of feedback errors over feedforward errors, the overflow turns on a front-panel OUT OF LOCK indicator and it initiates the transfer of the contents of the feedforward register, which now has valid data, into the feedback register. This is how the instrument achieves frame sync automatically.

Following start up, frame sync is required only when there has been a clock slip or when there has been a carrier loss. Each time frame sync is triggered, the clock slip totalizer is incremented one count.

This system is also used to detect the polarity of the data stream. If the data stream is inverted by the system under test, the output of the feedforward register will nevertheless have the proper polarity because both inputs to the exclusive-OR gate are inverted. The feedforward error detector would thus detect errors 100% of the time. If errors are counted 100% of the time, the control circuits switch an inverter into the data path.

The autopolarity system is locked up during a test interval to prevent bursts of errors from triggering polarity inversion.

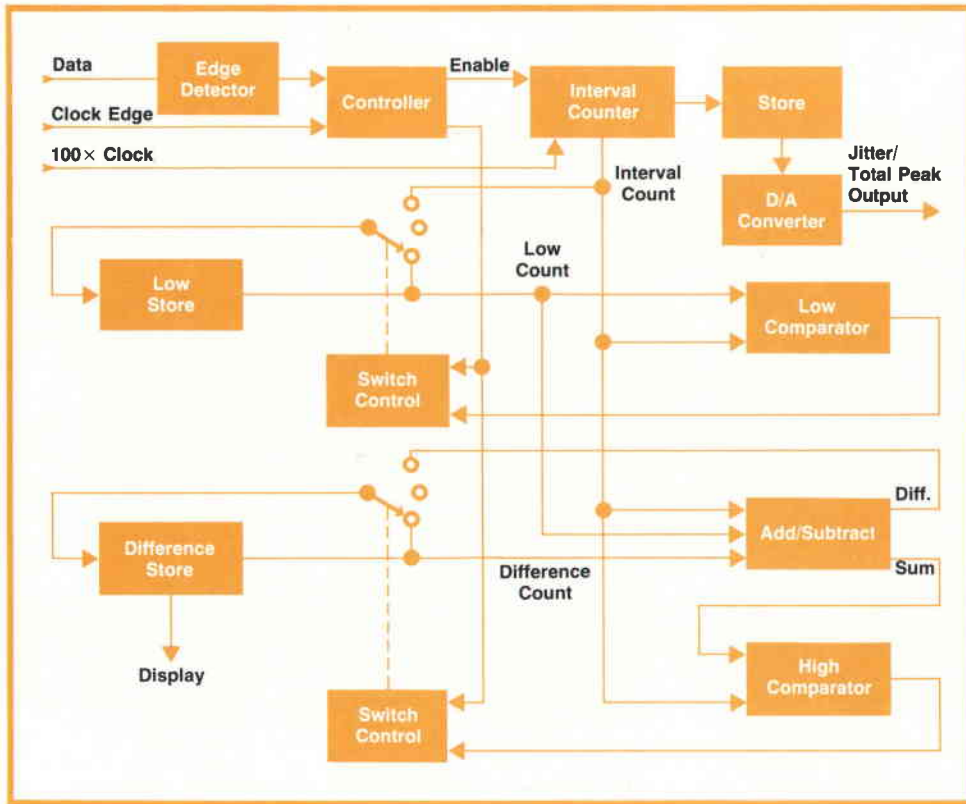


Fig. 7. Block diagram of jitter measurement circuit.

Jitter/Total Peak Measurement

Jitter is measured by counting $100\times$ clock pulses ($100\times$ faster than the clock rate) from a data edge to the clock edge, which normally occurs half way through the data bit period. The difference between the lowest and highest values counted during the test interval is a measure of jitter.

This is carried out by the system diagrammed in Fig. 7. Upon sensing a positive-going data edge, the edge detector generates a start pulse for the controller which in turn enables the interval counter to start totalizing $100\times$ clock pulses. The next clock edge stops the count, the exact count depending upon the position of the data edge with respect to the clock edge.

The count thus obtained is compared to the count in the low store register. If the count in the interval counter is the lesser of the two, it is loaded into the low store register in place of the count already there (the register was loaded with the first interval count at the beginning of a test).

The count in the interval counter is also compared to the sum of the counts in the low store and difference store registers. If the new count is greater than this sum, which represents the maximum count that has been received, the number in the low store register is subtracted from the new count and the result is loaded into the difference store register.

The difference register now contains a number that corresponds to jitter directly in terms of percent

of clock period (100 counts equals 100%). The contents of this register are displayed to give readings of jitter.

Total peak distortion (jitter plus bias) is measured by switching the edge detector to respond to both positive- and negative-going data edges. The number in the difference store thus reflects both the edge variations (jitter) and the relative positional difference between positive and negative edges (bias).

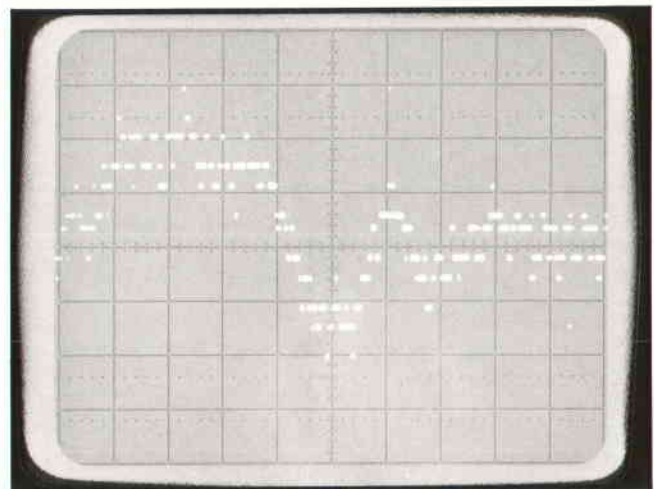


Fig. 8. Oscillogram of analog waveform available at JITTER/TOTAL PEAK output. The nature of the waveform helps determine the cause of the jitter (the waveform appears quantized because it is made up of discrete samples).

An additional feature of the system is that the interval counter contains continuously up-dated information about the position of data edges with respect to the clock. When the data-edge-to-clock count is complete, this information is converted to an analog voltage and presented at a front-panel connector, generating a waveform that corresponds to the movement of data edges with respect to the clock. The resulting waveform can be viewed on an oscilloscope, as shown in Fig. 8, as an aid in determining the source of the jitter. This output (JITTER/TOTAL PEAK) is calibrated so 1 volt out represents 10% distortion.

When the Analyzer is measuring total peak distortion, the oscilloscope's vertical deflection switches back and forth from the voltage corresponding to the positive-edge-to-clock interval to the voltage corresponding to the negative-edge-to-clock interval, tracing out two waveforms. The separation between waveforms is proportional to bias.

When the Analyzer is used with an external clock, the jitter measurement circuits are disabled since no $100\times$ clock would then be available. Jitter in synchronous systems, where an external clock most likely would be used, is usually less than 1% and is not a problem at the modem output. Jitter is primarily of concern with asynchronous systems where it may be as much as 20%.

Statistical Filter

A switchable filter is included in the incoming data path. Usually, the filter in the modem cleans up a noisy signal. Whether or not it is performing satisfactorily can be determined by comparing bit-error-rate measurements with the Analyzer's filter switched out to those made with the filter in.

The filter has to accommodate asynchronous bit frequencies from 75 to 9600 bps. As shown by the waveform in Fig. 9, analog filtering does not obtain reliable results so the filter used is a digital type that uses majority logic to decide whether a particular bit is a one or a zero. Each bit is sampled 100 times. Each time the sample is above the median threshold, it increments a counter. At the end of the bit, the comparator checks to see if 50 or more counts have accumulated. If so, that data bit is classed as a one. Otherwise it is a zero.

When the filter is disabled, the incoming data is sampled once in the center of each bit to determine whether it is a one or a zero.

Stable Clock

As mentioned previously, stable clock pulses are derived in the bit synchronizer. The heart of the bit synchronizer is a voltage-controlled 5.76 MHz LC oscillator that can be electrically tuned over a $\pm 0.5\%$ range. As in the case of the transmitter, dividers derive the various clock rates.

As shown in Fig. 10, the oscillator frequency is controlled by a phase detector, an RS flip-flop that is triggered on by a data edge and off by the next clock edge. This not only ensures that the instrument locks to the incoming bit rate, but it also places the clock edge midway in a bit period.

The output of the phase detector is averaged by a low-pass filter that is a compromise between stability (long time constant) and acquisition speed. Loop bandwidth is 3 Hz, which is well below the rate of change of jitter and other parameters to be measured with reference to the clock, but which permits fast acquisition from the operator's point of view.

The filter's time constant, however, would allow the oscillator to drift off frequency during the long pseudorandom sequence, which has long strings of bits in a row where no data edges occur. These would cause the phase detector to remain in either one of its two stable states, pulling the oscillator off frequency. Lengthening the filter's time constant to prevent drift from this source would seriously hamper acquisition speed.

This problem was solved by using a switch that disconnects the phase detector output, allowing the filter capacitor to retain its present voltage until the switch closes again. The switch is controlled by a comparator circuit that monitors the internal states of the input feedback shift register and turns off the

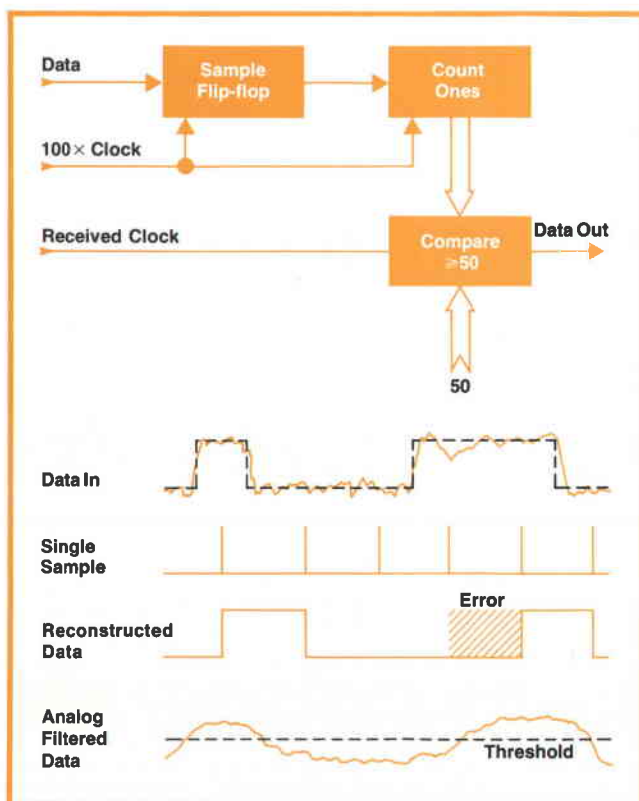


Fig. 9. Statistical filter reduces effects of noise.

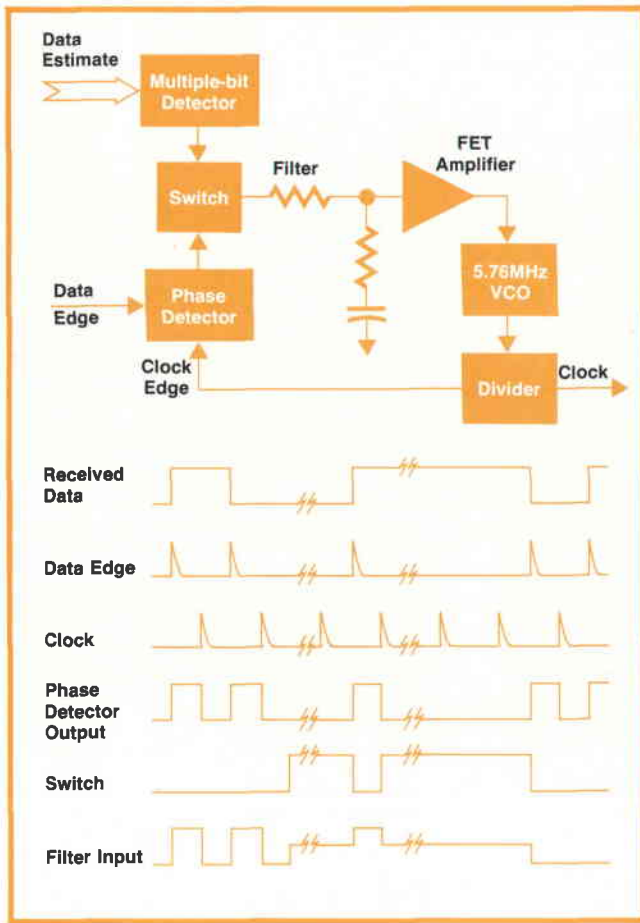


Fig. 10. VCO control loop.

switch whenever it detects that the register is about to output a long string of ones or zeros.

This arrangement reduces jitter during the long pseudorandom sequence from 15% or so to less than

1%. Another indication of the effectiveness of this circuit is that if the data input is removed, the oscillator remains in the correct phase for more than 5 seconds, equivalent to more than 375 bits at the slowest rate.

Autorange Control

The traditional way of displaying bit-error rate is as a number times 10 raised to some negative power ($A \times 10^{-x}$). This method is used in the Data Error Analyzer. It was also desired to display the count in progress which would indicate how much of the test interval had elapsed. This is accomplished by using the exponent in the display to indicate the number of data bits received in decade steps. At the conclusion of the test, the display then shows the overall bit-error rate properly ranged.

The autoranging system is shown in Fig. 11. Clock pulses are totalized in nine decade counters connected in tandem. The output of each of these counters goes to a selector. Initially, the output of the first decade is selected. As the clock count goes through 10, the first decade's output passes through the selector to increment the exponent counter. The exponent counter then shifts the selector to the next decade. This procedure repeats for each decade.

The count in the exponent counter is displayed continuously as the exponent. It is also compared to the number selected by the front-panel EXPONENT RANGE switch and when they become equal, the comparator stops the measurement.

In the automatic mode, the exponent counter receives a signal from the bit-error counter when 98 errors have been counted. It then stops the measurement when it receives the increment signal from the clock counter at the next decade change.

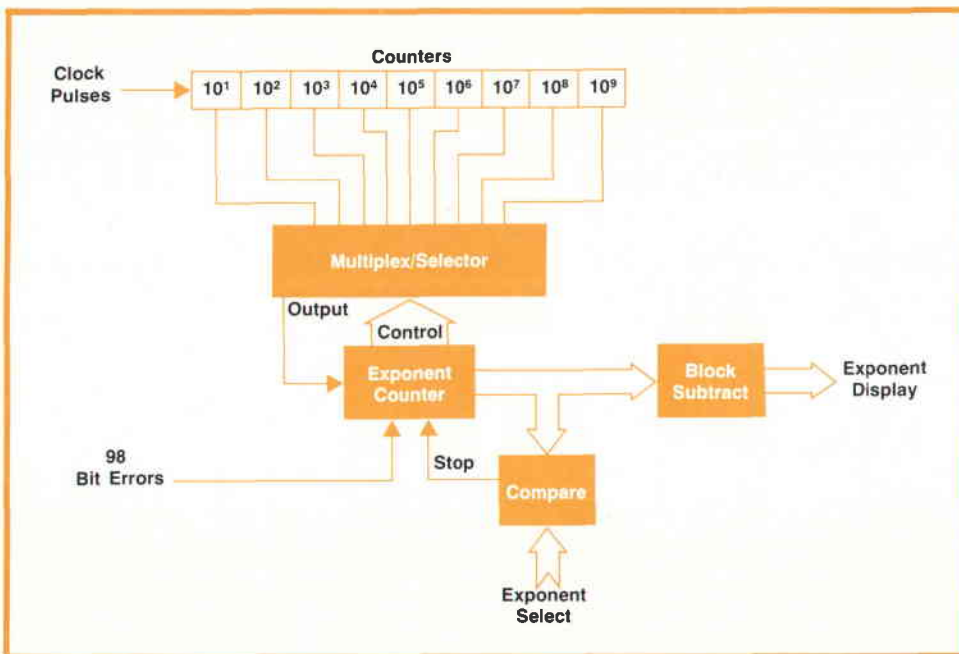


Fig. 11. Autorange circuit selects appropriate exponent to terminate test interval automatically.

The exponent counter's output passes through the block subtract circuit before display. This circuit subtracts 3 from the exponent count when the instrument is displaying block error rate, giving block er-

ror rate directly.

Acknowledgments

Appreciation is expressed to Al Knack for the innovative mechanical design, to Rick Vestal for many hours of patiently taking data on and with the Model 1645A, to Maxine Cheyney whose talents were essential to modularizing a complicated system, and to Eddie Donn whose creativeness was responsible for many of the basic ideas.

SPECIFICATIONS

HP Model 1645A Data Error Analyzer

Bit Rate

INTERNAL TRANSMITTER

BITS PER SECOND: selectable 75, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600.

CRYSTAL FREQUENCY: 5.78 MHz $\pm 0.03\%$; $< 0.01\%$ jitter.

INTERNAL RECEIVER (with bit synchronizer)

RATE: dc to 9.6 kbps.

TIME TO LOOP LOCK: 2 s max at < 0.01 error rate.

EXTERNAL TRANSMITTER and RECEIVER FREQUENCY: dc to 5 MHz.

Data Outputs/Inputs

REAR PANEL

INPUTS: backward channel data, external transmitter clock, and external receiver clock require TTL level; maximum input 5.5V.

OUTPUTS: bits lost and transmitter sync provide TTL levels; internal transmitter clock provides $> 2V$ into 50 ohms.

MULTIPIN CONNECTORS: RS 232C connector and interface levels for interfacing with standard communications systems. Printer output provides TTL level outputs in BCD 8421 code.

FRONT PANEL

INPUT: data input requires TTL levels; maximum input, 5.5V.

OUTPUTS: receiver sync, 16 bits before error, and event provide TTL levels; data output provides $> 2V$ into 50 ohms. Jitter/total peak analog output provides 1V p-p for 10% of p-p distortion from waveform causing jitter.

General

DIMENSIONS: 5.25 in H, 16.75 in W, 11.25 in D (133 x 416 x 286 mm).

WEIGHT: 22 lb (10 kg).

POWER: 115 or 230 Vac, 48 to 440 Hz, 150 VA max.

OPERATING ENVIRONMENT

TEMPERATURE: 0°C to +55°C.

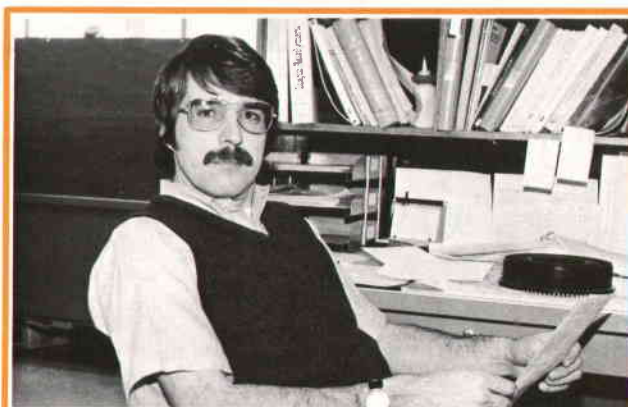
HUMIDITY: to 95% relative humidity at 40°C.

ALTITUDE: to 15,000 ft. (4600 m).

VIBRATION: vibrated in three planes for 15 minutes each with 0.010 in (0.25 mm) excursion, 10 to 55 Hz.

PRICE IN U.S.A.: 1645A, \$2150.

MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
1900 Garden of the Gods Road
Colorado Springs, Colorado 80907



Jeffrey R. Duerr

Joining HP in 1970 after two years in aerospace communications, Jeff Duerr initially worked on the 6940A/1900A programmable pulse generator system. Then, as project leader on the 1645A Data Error Analyzer, he combined engineering with the marketing research needed for developing an international product. He is now a sales engineer in the Colorado Springs Division. A native of Cleveland, Jeff earned a BSEE degree at the University of Rochester and an MSEE degree in communications from the State University of New York at Buffalo (1967). Jeff likes to spend weekends backpacking in summer and skiing in winter and he enjoys photography and blue-grass banjo picking all year around.

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