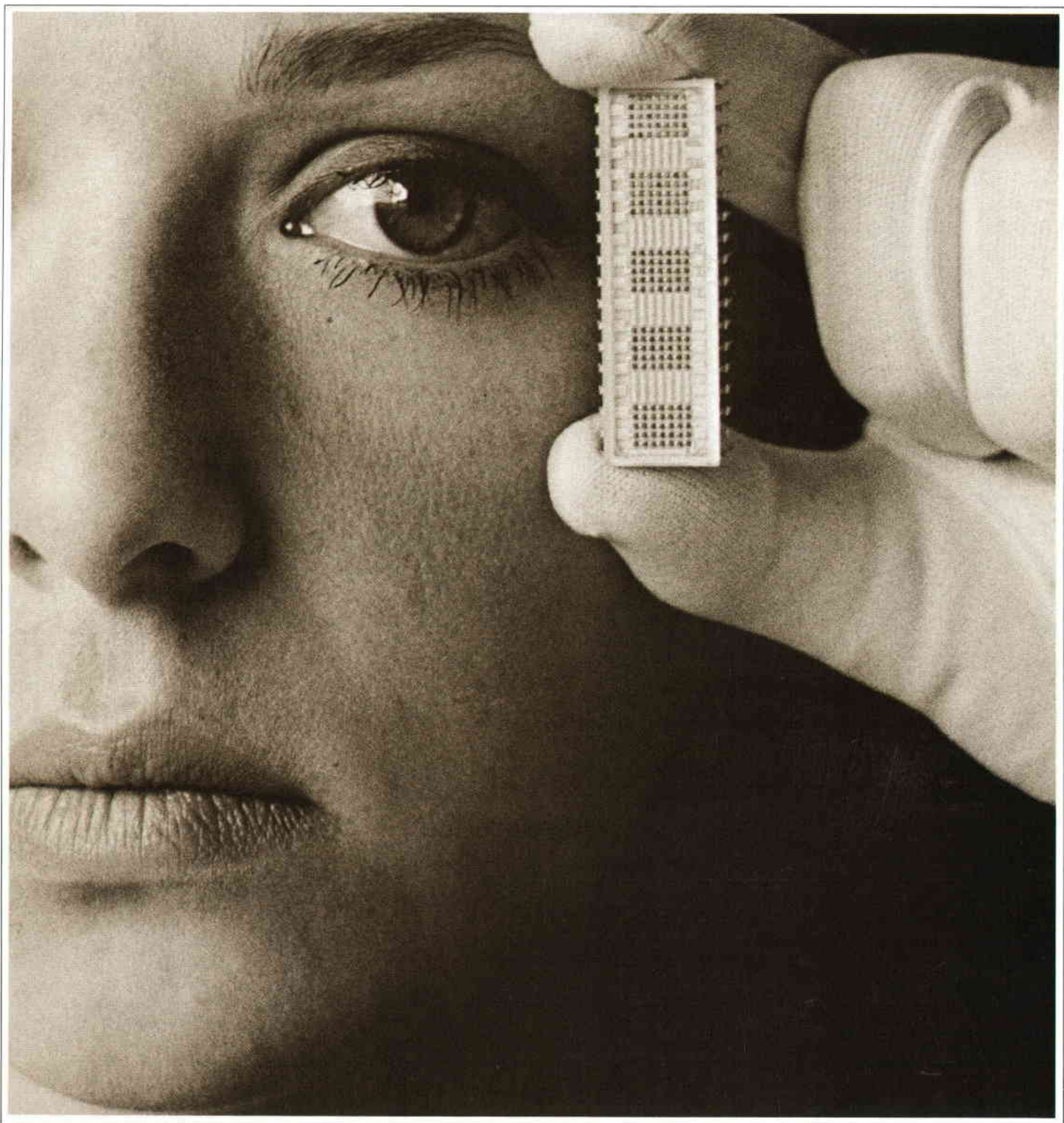


HEWLETT-PACKARD JOURNAL



JULY 1970

Solid-State Alphanumeric Displays

By Howard C. Borden and Robert L. Steward

'A DISPLAY IS AN INTERFACE BETWEEN A MACHINE AND A MAN. The man is affected by the optical characteristics of the display. Character font, size, color, viewing angle, brightness, and contrast all contribute to the subjective effect of the display on the man.'¹ It is implicit in this statement that the effectiveness of a display as a tool of man depends upon his success in coping with these characteristics in display design.

Display development must consider the effect on the system (or machine) imposed by the display. For example, system size, weight, complexity, response time, cost, efficiency, usefulness and competitive potential may be affected by limits imposed by the display. With the need for larger machine capability, it becomes necessary to add alphabetic and symbolic readout to numerics. It is then necessary to consider the display as a subsystem of the total system; to move from a static display (the numeric indicator, HP 5082-7000) to a dynamic display for alphanumeric indicators, Fig. 1.

In a dynamic display, the LED's are strobed (Fig. 2), that is, lighted in sequence at a rate so high that flicker is not apparent. Circuits are time-shared in this mode, which results in cost savings. Dynamic display is possible because of the fast response time of both the LED's and IC circuits.

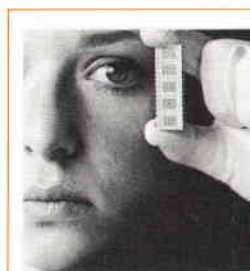
Display Devices

Many display devices are available. They use various types of light energy mechanisms in their operation. Most are limited by using readouts made up of seven segments (or bars). A few provide sixteen-bar segment alphanumeric readout, Fig. 3, and some have a 5×7 dot matrix readout for alphabetic, numeric and limited symbolic readout. The major types include (1) gas plasma, (2) tungsten lamp direct view, (3) tungsten lamp light-pipe

coupled, (4) tungsten lamp projection, (5) shadow-mask electron-beam projection, (6) low voltage phosphor-coated anode devices, (7) electric field excited EL panels, (8) liquid crystal, and (9) cathode ray tubes (CRT's).

The obvious question is, 'With all of these, who needs injection luminescent light emitting diodes?' In looking at the list, the display designer becomes aware of the fragile nature of all of these devices. The need for high voltage to operate many of them limits size reduction. In addition, they are not compatible with integrated circuits, and in many cases there is a substantial compromise with good optical characteristics.

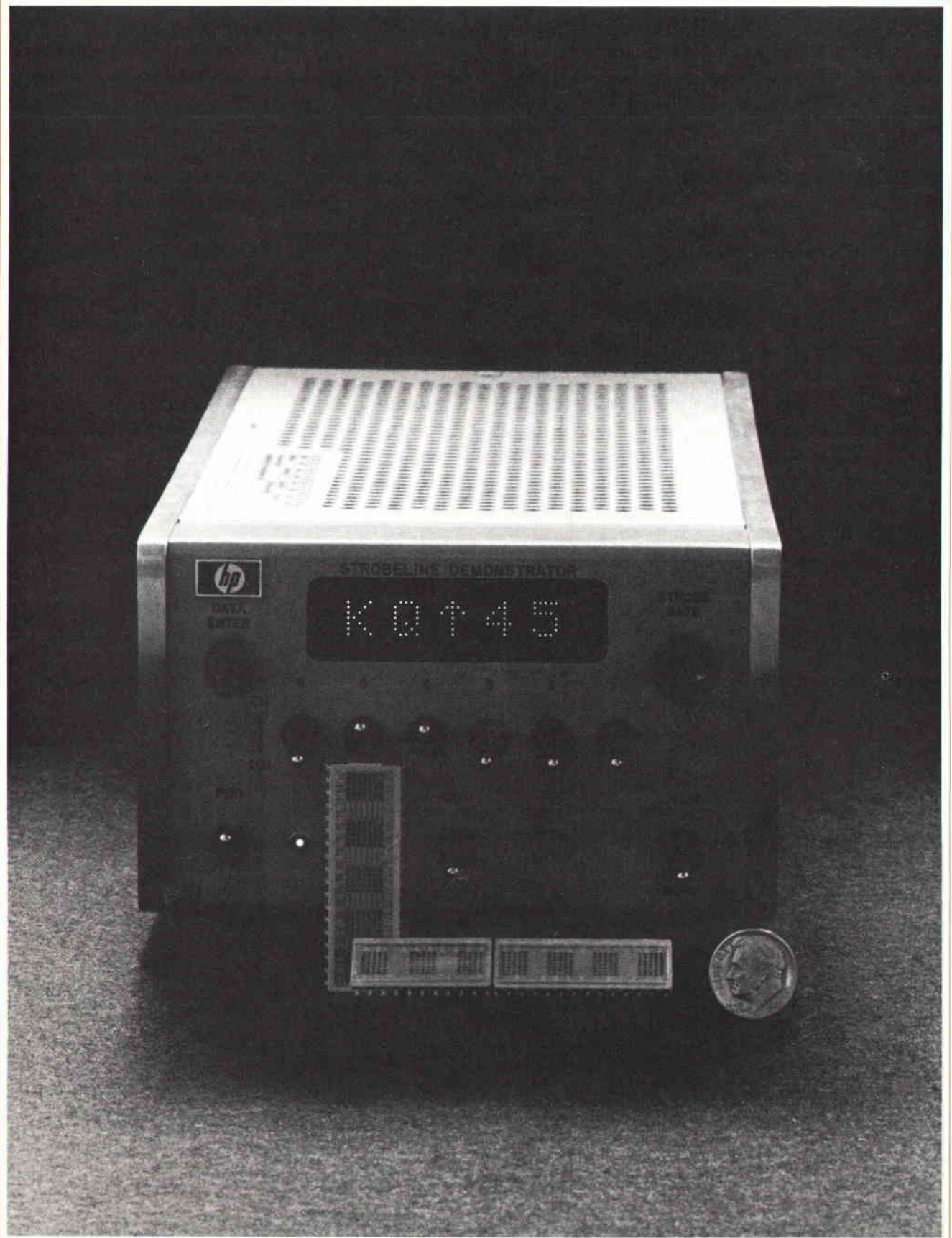
Without question the CRT is the best answer to display flexibility. It is towards matching the CRT capabilities that solid state display development is directed. There is



Cover: Inspector critically eyes solid-state alphanumeric display module. In Dual In-Line Package mounting, five characters are spaced three to the inch. Each character is a 5×7 array of 35 light-emitting diodes.

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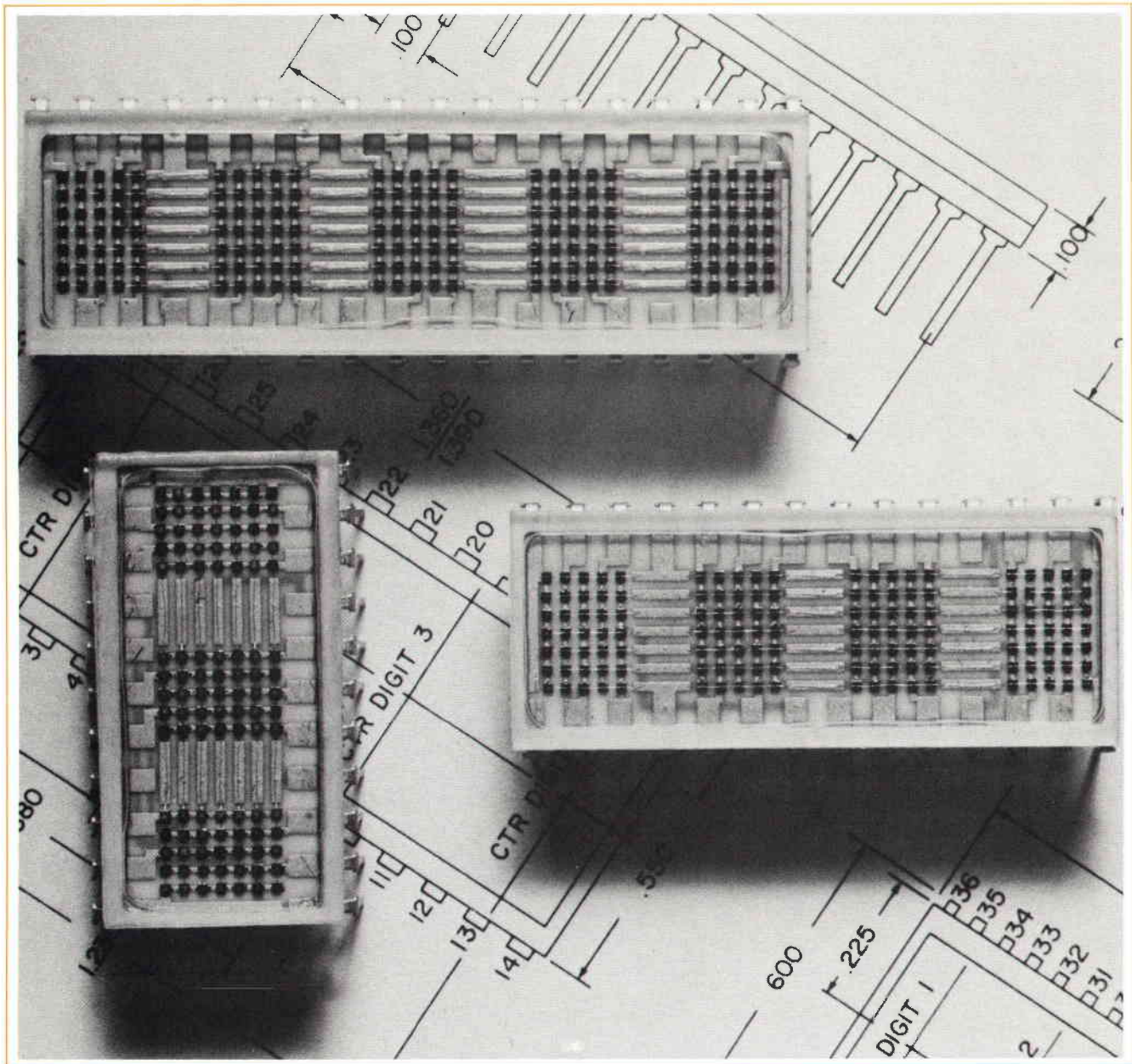


Fig. 1. Alphanumeric indicators are made in groups of three, four and five.

little doubt that this target can be realized, in spite of some problems with cost, power, color limitations, and electrical accessing.

These problems are not formidable. First, cost is relative. For example, tracing the evolution of the semiconductor industry from the first point contact germanium transistor from its laboratory introduction to the 'penny a point' current silicon memory pricing will strike down most concern for cost. Second, the power requirement for the LED is falling as its efficiency is improved. In three years, LED drive current has dropped from

40 mA to 2.5 mA for the same emitted light.* Materials other than the present Gallium Arsenide Phosphide (GaAsP) used in the HP displays promise luminous efficiencies at least two orders of magnitude higher than the 2×10^{-4} of present materials. Colors other than red will also be possible. Achieving lower drive voltages, faster response times, and better ruggedness and reliability of LED's coupled with nearly ideal optical characteristics provide real challenge to the designer of solid state display systems.

*Present luminous efficiency is approximately 75 fL/A.cm².

Alphanumeric Display

The HP 5082-7102 Alphanumeric Display, Fig. 4, is a small, rugged display device designed as a flexible dynamic display in a GaAsP solid state readout. The package, a multilayer ceramic design, is a standard Dual-In-Line (DIP) configuration for easy mounting in inexpensive plug-in type sockets, or for direct insertion into printed circuit boards. Pins are arranged in two lines of 0.600-inch separation, with the pin-to-pin separation at 0.100 inch—standard printed circuit board line and hole spacing. Also, the packages may be assembled end-to-end with no change of the three-to-the-inch character spacing between packages. While the HP 5082-7102 has five characters per package, packages with three and four characters are also available. A thermal diffuser built into the package takes care of the heat transfer problem. The use of buried layer metallization in the package permits electrical accessing in a very compact package. The display system concept, then, derives from the use of this display package with integrated circuit signal processing and solid state memory.

Strobed Dynamic Display System

Dynamic operation of the display has been developed to combine presently available integrated circuits, including the 2,240 bits of memory needed to provide sixty-four characters of 5×7 matrix size in large scale integrated Read Only Memory (ROM) in a practical electrical drive configuration. All of the IC's needed for embodiment of the system are commercially available. Dynamic operation reduces the number of pins on the display package to a practical number. At the same time, the user has a choice of a large number of designs to drive the display, depending upon his needs in terms of character font, speed, intensity, electrical interfacing with other parts of the total system, as with ECL, TTL, or MOS logic. Sharing of timing circuits with functions other than display is possible.

Each basic character or array of the alphanumeric display is a 5×7 matrix of LED's. These are electrically accessed in row and column fashion; there are five connections for the five columns (the LED cathode connections), and seven connections for the seven rows (anodes), Fig. 5. The seven rows of each array of the display are connected in parallel, so that all arrays may be driven at one time. Thus, for any size of display the number of electrical leads for the display package will be $7 + 5N_A$, where N_A is the number of arrays in the display, 5 the number of columns in an array and 7 the number of rows.

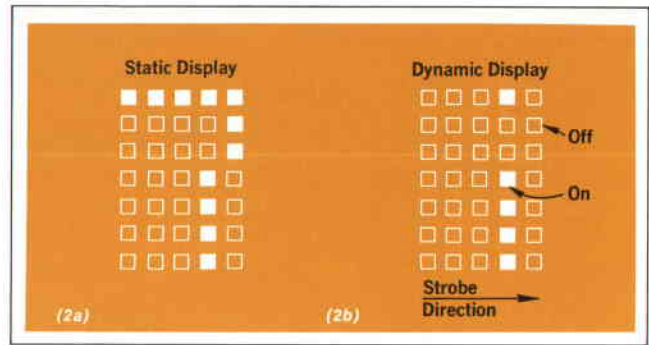


Fig. 2. In a static display (A), the diodes are on continuously. Characters of a dynamic display are formed by pulsing one column at a time (B).

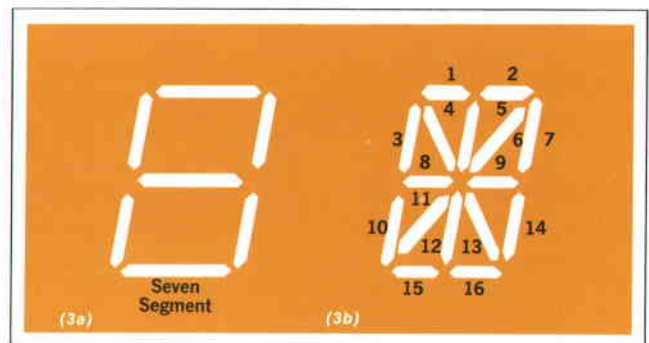


Fig. 3. Only a limited number of characters can be generated by seven bar (A) and sixteen bar (B) segment displays.

With simple X-Y accessing of a matrix, only time sharing will provide control of all points of the matrix. In the case of the HP display, any subset of diodes can be lighted, Fig. 6. Recommended operation for the 5082-7102 alphanumeric display is to scan the arrays from top to bottom, row by row, with the encoded signal for each row of all characters appearing simultaneously. This is vertical strobing, Fig. 7. A very important feature of vertical strobing a 5×7 array versus horizontal strobing is that the display 'on' duty cycle is about 14%, and the addition of many arrays of display need not significantly change this duty cycle. (See 'The Mathematics of Strobed Arrays,' inset.) Because of the speed of integrated circuits, the expensive ROM needed to provide conversion from the encoded (ACSII, EBCDIC, etc.) input signal may be shared with a number of arrays, materially reducing the display system cost.

Referring to Fig. 8, a block diagram of one electrical driving system, one can follow the operation of a display from a keyboard. The basic functions are:

1. Input keyboard, with six line ASCII output,
2. Master clock and timing circuits,

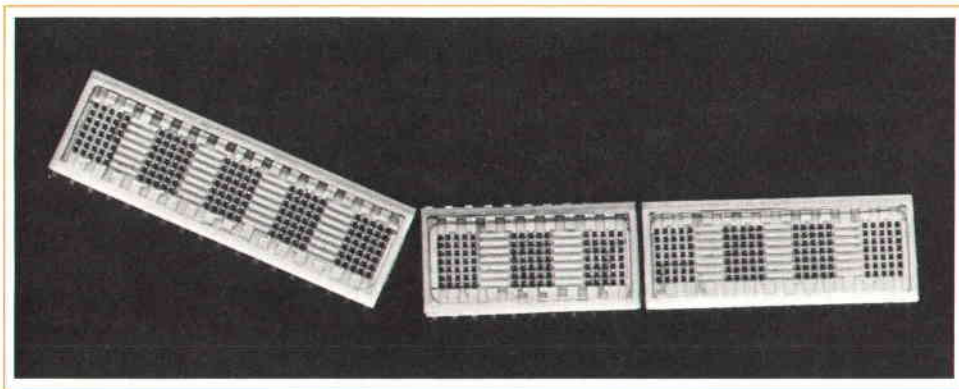


Fig. 4. HP alphanumeric display packages can be assembled end-to-end and a three character per inch spacing maintained.

3. Array select circuit (distributes ASCII code to input storage buffers),
4. Input storage buffers (holds display message in ASCII code form),
5. 2240 bit ROM (converts 6-line ASCII to 5-bit single character row information),
6. Output storage buffers (holds a five bit word for each display character, one row at a time),
7. Column drivers (provide current pull-down capability and current regulation for all columns of the display),
8. Row drivers (provide drive power for sequential operation of each row of all arrays),
9. LED display (HP 5082-7102).

Vertical Strobing System Operation

Operation of this system is as follows:

1. Characters are selected by means of the keyboard. Depressing a key provides a system timing signal and a six-bit ASCII coded output. Obviously, this input might alternatively be a six-bit parallel input from a driving system or six bit serial input converted to parallel with a serial in, parallel out shift register.
2. The Master Clock and Timing Circuits synchronize the display system, and in many cases could be tied in with the timing of the driving system, a computer, counter, or other signal source. The timing circuits set the rate at which the display operates, including the breakup of the character information into individual row words for each character. As the LED display does not contain memory, and the individual diodes have very fast optical response to electrical currents (approximately 10 nanosecond rise and fall times), the display is continually refreshed as in a CRT display, but vertically row by row rather than with a point-scanning beam. At refresh rates above 100 Hz, flicker is indiscernible. However, if the display is subject to vibration during operation, the field rate should be increased to 1 to 10 kHz as required to avoid character breakup.

3. The Array Select Circuit accepts the asynchronous keyboard output timing pulses and enables the next Input Storage Buffer to accept a new input.

4. The Input Storage Buffers are enabled sequentially left to right #1 to #N_A, with #1 following #N_A. It is a simple matter to erase all characters and start at #1 for a new message. The display message is available at the input storage buffers in 6 bit ASCII format at all times and is read from them 6 bit parallel, character serial form.

5. The heart of the system is the 2240 bit, character-generating ROM. This 'reference table' of fixed information allows one to 'look up' the 5 × 7 character font data for any one of 64 standard alphanumeric characters. The font information is outputted, bit parallel, in a five bit word, one row at a time; the exact row is determined through the ROM's Row Select input. The ROM's 1 microsecond response time is fast enough for loading of the Output Storage Buffers for a 25 character display at a refresh rate of 1 kHz, or up to 100 characters at 250 Hz.

6. The ASCII coded message in storage is brought to life by generating, storing, and displaying the character format information one row at a time. Thus, row #1 for all characters is generated and stored at the Output Storage Buffers in a character sequential, bit parallel manner. Following the *display* of this data on row #1 of the LED arrays, row #2 information is obtained from the ROM and stored. Upon loading of the last Output Storage Buffer, row #2 of the message is presented on the second row of the display. The remaining rows are presented analogously. Following row #7, the process is repeated. Using row #1 as an example, the exact operational sequence is: the ROM accepts character #1 ASCII input from Input Storage Buffer #1 and outputs the character #1, row #1 five bit word to Output Storage Buffer #1; accepts display character #2 ASCII input from Input Storage Buffer #2 and outputs a five bit word

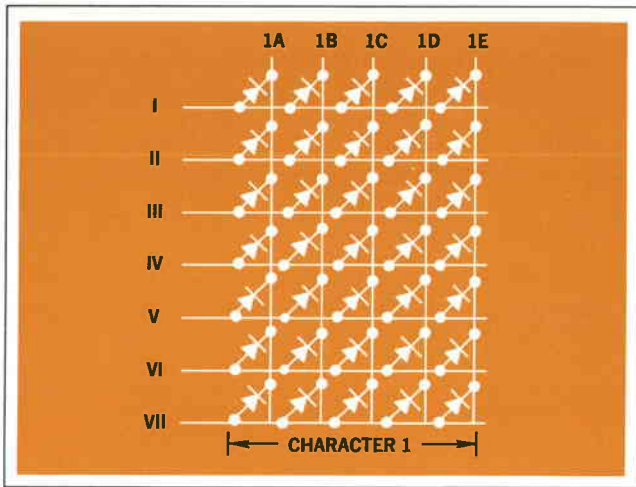


Fig. 5. A single character of an HP alphanumeric display showing the electrical arrangement of the light-emitting diodes.

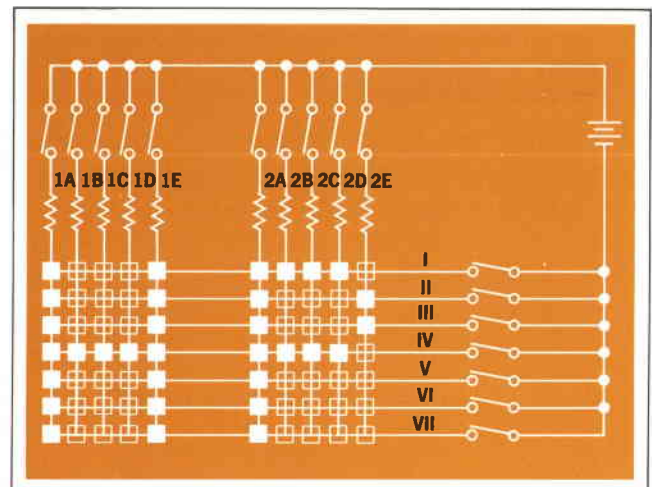


Fig. 7. Vertical strobing forms characters by time sequentially selecting rows and energizing the correct diodes in each column.

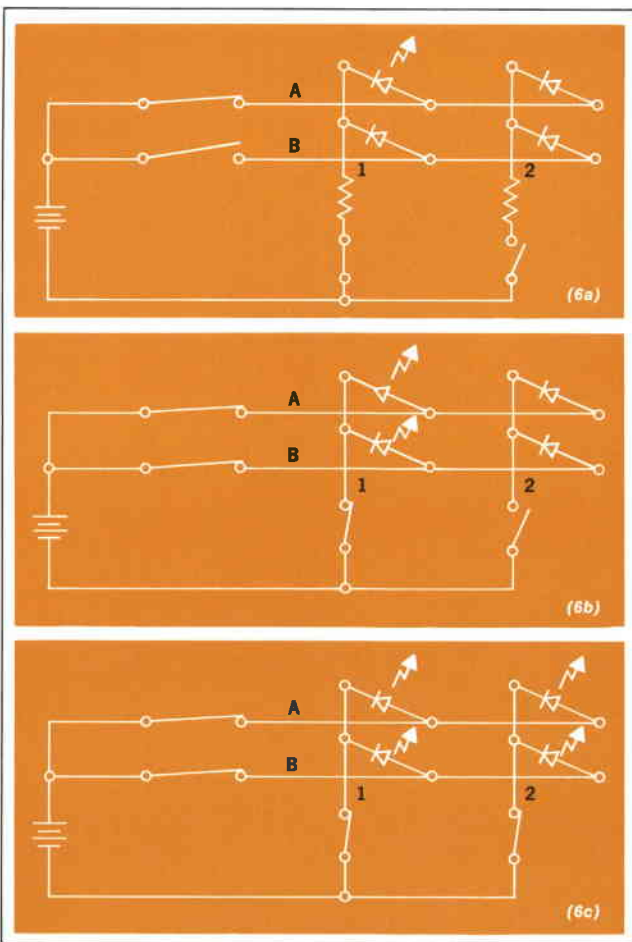


Fig. 6. Individual control of each diode in the matrix is not possible without using a strobing technique. In (A), simple switching will light A1; in (B) A1 and B1 can be lighted. In (C), it is not possible to light only A1, A2, and B1. B2 also lights.

representing character #2, row #1 to Output Storage Buffer #2; . . . ; accepts character # N_A ASCII input from Input Storage Buffer # N_A and outputs the character # N_A , row #1 five bit word to Output Storage Buffer # N_A . Row Driver #1 and the Output Storage Buffers are then enabled to supply LED drive current for the desired display time. The data in the Output Storage Buffers determines which column drivers will provide a path to ground and, hence, which LED's of row #1 will be lit. Display tradeoffs available to the designer are discussed in the inset.

7. Column drivers with current limiting resistors can easily sink the 35 mA peak pulse current at each column. Since a row is turned on only $\frac{1}{2}$ of the time, the peak drive current per diode must be seven times the desired average current level of 5 mA. Since only one row is driven at a time, the resistive current limiting is adequate. The uniformity of the forward voltage characteristic of the LED's permits a low voltage compliance range, with resulting small power consumption in the current limiting resistors.

8. Row Drivers are required to drive as many as the full number of columns in the display. As this may be as much as an ampere for a five array display, the saturation voltage of the switching transistor must be considered, along with the driving current requirement for saturated operation. However, it is not hard to find adequate, inexpensive transistors or core driver blocks. For luminous intensity control it is recommended that a variable duty cycle be used to permit a wide range of brightness with good overall uniformity.

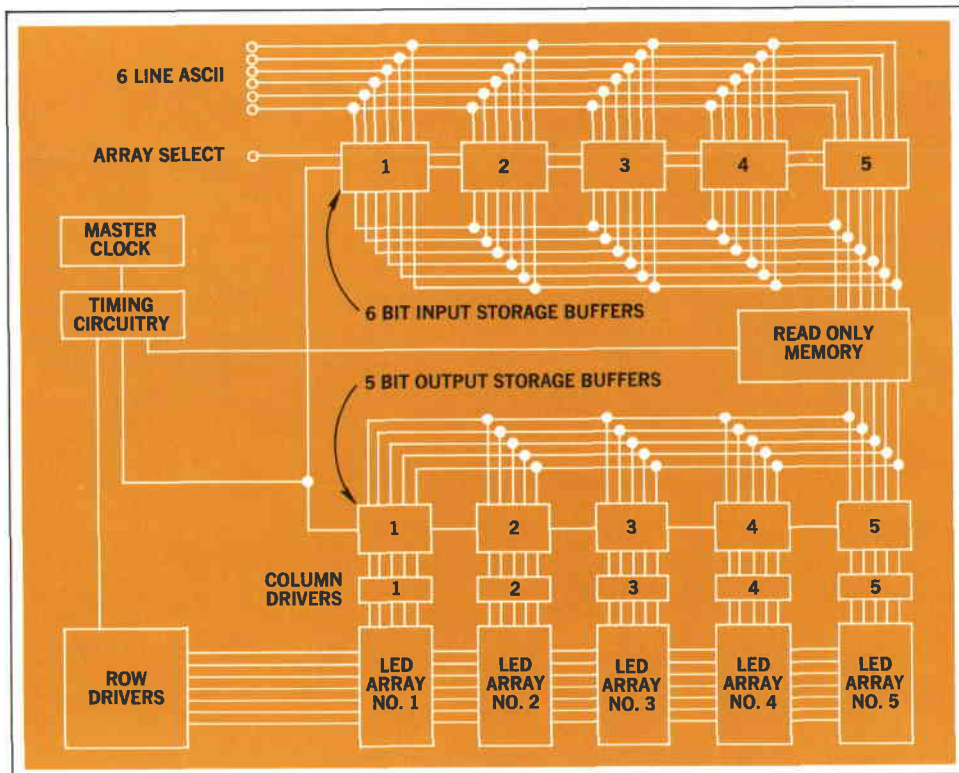


Fig. 8. Block diagram of vertical strobing of LED arrays.

Conclusion

The use of a solid-state light-emitting display for alphanumeric is a commercial reality. Economics of this type of display are presently most favorable for limited numbers of arrays, say, less than 20, or where operation is under adverse environmental conditions, where space is limited, or where solid state reliability is needed. Semiconductor prices have been dropping about 30% per year. It is likely that solid-state displays will follow this pattern. □

Reference

[1] Howard C. Borden and Gerald P. Pighini, 'Solid State Displays' **Hewlett-Packard Journal**, February 1969.

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- [2] R. A. Burmeister, Jr., G. P. Pighini, and P. E. Greene, 'Large Area Epitaxial Growth of GaAsP for Display Applications,' Transactions of the AIME.
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SPECIFICATIONS

(at 25°C unless otherwise specified)
HP Models 5082-7100—5082-7102
Solid State Alphanumeric Indicator

POWER DISSIPATION (at 50 fL 'Apparent' luminosity*)
 Character B (20 diodes)
 All 35 diodes lit

PEAK FORWARD CURRENT (per diode)

OPERATING AND STORAGE

Temperature

REVERSE BREAKDOWN VOLTAGE AT 10 A

LUMINANCE OF EMITTING SURFACE OF DIODE AT 10 mA
 (diode average)

* 'Apparent' refers to the subjective equivalent luminance value. The display output is pulsed.

TYPICAL CHARACTERISTICS

Luminance of emitting surface of diode at 10 mA
 (diode average)

Forward Voltage at 10 mA

Peak Wavelength

Spectral line halfwidth

PRICE: Per character

1-9	\$70
10-99	\$55
100-499	\$45
500-999	\$35
1000 and over	\$30

MANUFACTURING DIVISION: HP ASSOCIATES
 620 Page Mill Road
 Palo Alto, California 94304

The Mathematics of Strobed Arrays

Many tradeoffs are available to the design engineer in his search to optimize the display system to his needs. In this discussion, assume a five column by seven row array.

The parameters involved are:

- N_A = the number of arrays in the display.
- r_F = field rate, the refresh rate of the whole display.
- t_F = field time, the cycle time for the whole display; $(1/r_F)$.
- t_L = row load time, the time spent loading all the Output Storage Buffers with a row of character font information.
- t_D = row display time, the time spent displaying a row of character font information.
- t_{BL} = buffer load time, time required to load a 5-bit word into an Output Storage Buffer.
- t_{ROM} = ROM response time, the propagation delay time

of the ROM.

d_R = row duty cycle, the time spent loading and displaying a row of information, the percent of time used to display; $\left(\frac{t_D}{t_L + t_D}\right)$

d_D = display duty cycle, percent of the field time that any given row driver is enabled; $\left(\frac{t_D}{t_F} \text{ or } \frac{d_R}{7}\right)$.

For a system containing one ROM and one set of seven row drivers, the following equations can be derived:

$$d_R = (1 - 7r_F N_A t_{ROM}) \times 100$$

$$d_D = \frac{1 - 7r_F N_A t_{ROM}}{7} \times 100, \text{ (in percent)}$$

For example, if we wish a 90% row duty cycle, a 200 Hz field rate, and using a ROM with 1 μ s response time, we could display up to 72 characters.

Howard C. Borden



Howard Borden's background includes study of mechanical engineering at Massachusetts Institute of Technology and Electrical engineering at the University of California at Berkeley. He graduated from the U.S. Navy Materiel School in 1943 and received his BA degree from Stanford University in 1961.

Howard was with Stanford Research Institute for almost 10 years engaged in development of video systems. He also worked in industry developing large area, solid state, photo arrays. Since joining HP in 1966, Howard has been involved with integrated circuits, injection luminescent displays and optical data retrieval techniques. He is presently Senior Display Scientist.

Robert L. Steward



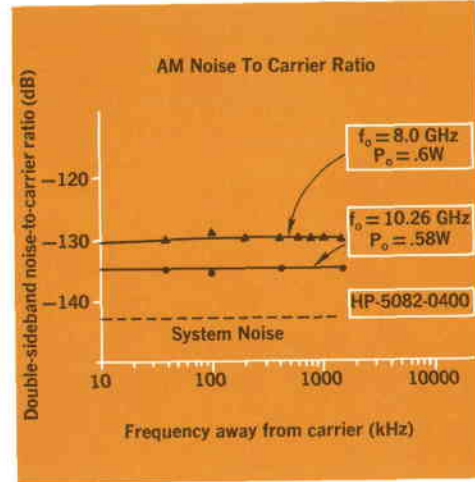
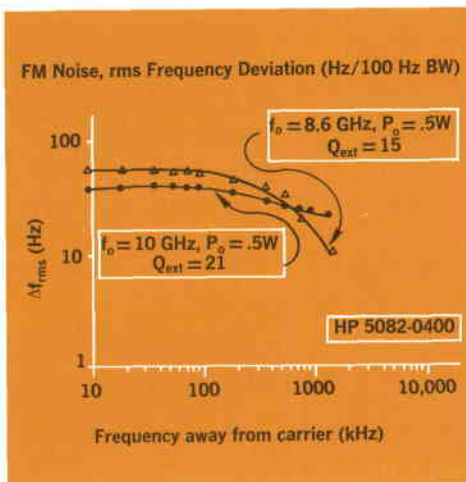
Bob Steward received his BSEE from San Jose State College in 1968, and his MSEE from Stanford University in 1969. He joined Hewlett-Packard immediately upon graduation.

Bob is an integrated circuit engineer and has worked on memory and control circuits for solid state displays. He worked on the development of the decode, drive and memory circuitry used with the HP alphanumeric displays.

Among Bob's society memberships are IEEE, Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi. He is also a Graduate Fellow of the National Science Foundation, 1968-1969, and is in Who's Who in American Colleges and Universities, 1967-1968.

Noise in IMPATT Diodes

The two illustrations, right, omitted from the article on IMPATT diodes in the May issue (Fig. 11), show FM and AM noise in Hewlett-Packard IMPATT diodes operated well below the power saturation level (measurement bandwidth for both figures was 100 Hz). Experience has shown FM performance to be even better in higher-Q circuits; for example in cavities with Q's on the order of 100 to 200, FM noise is typically 7 Hz in a 100-Hz bandwidth at X-band, comparable to klystrons.



Adding More Precision to Spectrum Analyzer Measurements

Augmented with a combination tracking signal generator and counter, the spectrum analyzer becomes a swept measuring system of great frequency precision and dynamic range.

By Patrick J. Barrett, Robert R. Hay and Paul G. Winninghoff

ACCURATE MEASUREMENT of the frequency of low level RF signals, especially when intermixed with higher level signals, has always been difficult and sometimes impossible. Equally challenging have been frequency response measurements of very narrow-band devices over a wide dynamic range. A new instrument which incorporates a tracking generator and a counter (HP Model 8443A) combines with the HP Model 8552/8553 Spectrum Analyzer to make such measurements simple in the 100 kHz to 110 MHz range. The system that emerges adds up to more than the sum of its parts. It performs the functions of many test systems.

Swept Transmission Test Set

Transmission is measured over more than 120 dB dynamic range with 0.1 dB resolution. There is a movable frequency marker. Frequency resolution is 10 Hz.

Swept Reflection Test Set

Return loss measurements may be made to more than 40 dB. Again, resolution is 0.1 dB in amplitude, 10 Hz in frequency.

Synthesizer with Tracking Detector

With peak-to-peak residual fm under 0.1 Hz and a full-screen scan width as narrow as 200 Hz, the frequency response of narrow-band devices may be seen with 120 dB dynamic range. Frequency is shown with ± 10 -Hz accuracy.

Selective Frequency Counter

Maximum sensitivity is -140 dBm—20 nanovolts. Selectivity is 10 Hz, resolution 10 Hz, and accuracy ± 10 Hz, resolution 10 Hz, and accuracy ± 10 Hz, even in the presence of other signals as much as 70 dB greater. Measurements thus may be made which are otherwise very difficult, if not impossible.

Spectrum Analyzer

As a spectrum analyzer pure and simple, it is calibrated in amplitude from -140 dBm to $+10$ dBm, with

flatness of ± 0.5 dB, resolution from 10 Hz to 300 kHz, and displayed dynamic range 70 dB.

Using the System

The 8443A Tracking Generator/Counter will indicate the frequency of any signal that may be displayed on the Spectrum Analyzer CRT; to select a signal the operator simply positions an intensified marker on the desired signal using the marker position control, and the counter displays the marker frequency.

The Tracking Generator and Spectrum Analyzer also form a swept measurement system since the Tracking Generator output signal exactly tracks the input tuning of the Spectrum Analyzer. In essence it is a sweeper which tracks a receiver. The system will display the amplitude response of any device placed between the Tracking Generator output and Spectrum Analyzer input.

The tracking generator is available alone, without the counter, as HP Model 8443B. Measurements made with the resulting system retain the amplitude range and frequency stability of the 8443A, but of course the frequency information available will be only that which may be derived from the spectrum analyzer. Counter circuitry can be added at any later time to an 8443B, converting it into an 8443A.

The counter section of the 8443A measures the frequency of the tracking signal by stopping the Spectrum Analyzer scan at some predetermined point in the scan, counting the frequency, then resuming the scan. When the scan is stopped, an intensified marker appears on the CRT where the scan stopped. The marker can be positioned with the MARKER POSITION control. In this way, the counter is able to measure the frequency of any signal appearing on the Spectrum Analyzer CRT. The MARKER POSITION control can be turned into a manual sweep control, by placing the counter in the SCAN HOLD mode. Using this mode the operator can



Fig. 1. *Combination Tracking Generator and Counter (above) mates with Spectrum Analyzer (below) to form powerful swept measuring system.*

slowly trace out any signal and carefully study details of interest, while the counter is continually updating the frequency readout.

High-resolution frequency response measurements can be made with the system using the calibrated output attenuators on the 8443A and the LINEAR (or alternatively the 2 dB LOG) display mode on the Spectrum Analyzer. High dynamic range is available in the 10 dB LOG display mode and the Spectrum Analyzer IF attenuator may be used to extend the display range of a measurement.

There are many applications for such a system. In the communications field, for example, it will check communication channels by measuring carrier and modulation frequency and level, and by locating spurious, harmonic, and interfering signals. There are additional applications in the RFI analysis, spectrum surveillance, and laboratory design fields.

Using the system for swept measurements one can characterize filters, amplifiers, attenuators, and systems comprised of these elements, such as IF strips. This single system can measure the center frequency, flatness, bandwidth, shape factor, and pass/stop band ratio, for example, in filter testing. With a directional bridge, return loss or reflection coefficient as well as transmission measurements can be made with the system. Thus the system should find usefulness not only in laboratory design but also in production testing and field service.

Theory of Operation — System Description

The 8552A/8553B Spectrum Analyzer is a triple conversion swept receiver calibrated in frequency and amplitude. As shown in the block diagram (Fig. 2) the input is mixed with a 200–310 MHz signal to convert it up to the 200 MHz first IF. The first local oscillator (LO) is swept for scan widths of 500 kHz or greater, enabling the Spectrum Analyzer to display as much as 100 MHz of the whole 1 kHz to 110 MHz band at one time. The crystal-controlled 150 MHz second LO down-converts the signal to 50 MHz for the second IF. The 50-MHz signal is then mixed with the 47-MHz third LO to produce 3 MHz. For scan widths of 200 kHz or less the first LO is tuned to a fixed frequency and the third LO is swept. For optimum frequency stability the first LO can be phase locked to an internal crystal controlled reference at 100-kHz intervals, when the third LO is being swept. The 3-MHz signal which results from mixing the 50-MHz and 47-MHz signals passes through the bandpass filters and logarithmic amplifier in the third IF to the detector, and the output of the detector is displayed on the CRT. The 3-MHz bandpass filters determine the receiver bandwidth; they are selected by a front panel control on the Spectrum Analyzer.

The Tracking Generator recombines the signals from the Spectrum Analyzer to produce an output signal which exactly tracks the tuned frequency of the Spectrum Analyzer. As may be seen from the block diagram a 3-MHz

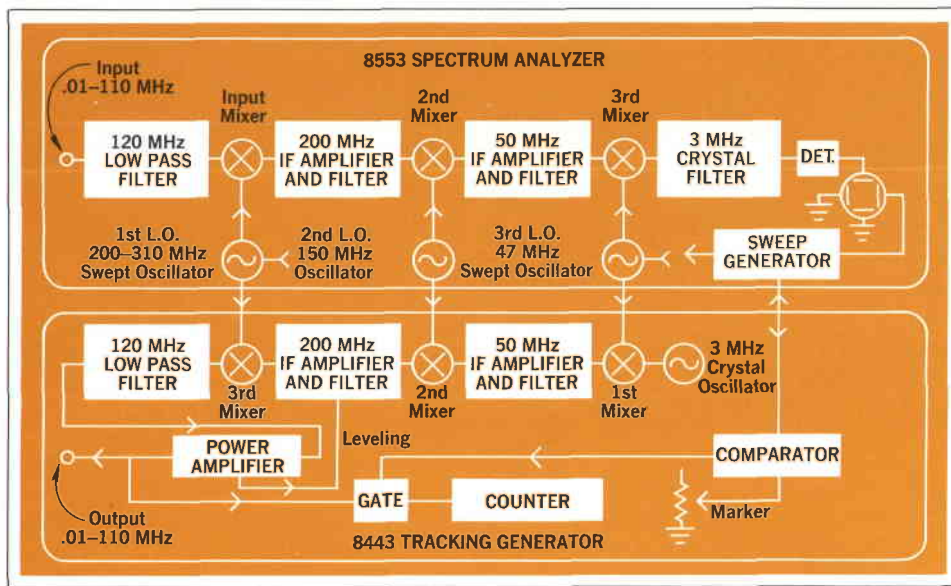


Fig. 2. Block diagram of Tracking Generator/Counter with Spectrum Analyzer.

signal from a crystal oscillator in the Tracking Generator is mixed with the 47 MHz LO signal from the Spectrum Analyzer to produce 50 MHz. This signal in turn is up-converted to 200 MHz by the 150-MHz LO signal, and the 200-MHz signal is mixed with the 200–310 MHz first LO to produce the tracking signal. The tracking signal is amplified to a level of +10 dBm; that signal is made flat within ± 0.5 dB over the frequency range by an automatic level control (ALC) circuit. Various output signal levels can be selected with the output attenuators.

RF Section

One of the most critical components in the RF portion of the 8443A is the 3-MHz crystal oscillator. If the Tracking Generator output signal is to track the Spectrum Analyzer accurately, the 3-MHz oscillator's frequency must match the center frequency of the 3-MHz IF crystal filters within a few hertz. The oscillator was designed around the same crystal that is used in the IF filters to minimize tracking errors from thermal drifts; in consequence, the crystals in both instruments drift in the same direction at approximately the same rate. In addition, there is some frequency adjustment capability in the oscillator to compensate for slight variations in the actual center frequencies of the crystals. The equivalent circuit of a crystal is a series RLC circuit. If a capacitor is connected in series with the crystal, it will shift the resonant frequency higher; similarly a series inductor will shift the frequency lower. To permit an adjustment of approximately ± 150 Hz about the center frequency of the crystal, the 3-MHz oscillator has a variable capacitor and an inductor in series with the crystal, as illustrated in the simplified schematic in Fig. 3. The 3-MHz oscillator is

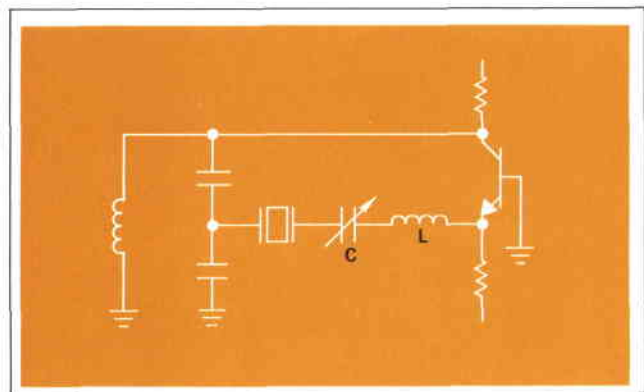


Fig. 3. 3-MHz Crystal Oscillator.

aligned with the center frequency of the 3-MHz IF filters in the Spectrum Analyzer by connecting the Tracking Generator output to the Spectrum Analyzer input and then adjusting the variable capacitor for maximum signal level indication on the Analyzer CRT. This adjustment is the TRACKING ADJUST, accessible from the front panel.

All three mixers in the Tracking Generator are doubly balanced and are similar in design to those used in the Spectrum Analyzer. The LO signal to each mixer is supplied by a buffer amplifier which provides isolation between the Spectrum Analyzer and Tracking Generator, to prevent spurious mixing products from getting into the Analyzer. The amplifiers also boost the signal to a level high enough to drive the mixers, since the signals come out of the Analyzer at a relatively low level; and the amplifiers provide the necessary 50-ohm terminations for the LO lines from the Spectrum Analyzer.

Product Design

By William H. Bull

The primary objectives of the product design of the 8443A were 1) to build an instrument that can be efficiently manufactured, 2) to make it aesthetically compatible with the 8552/8553 Spectrum Analyzer, 3) to shield it effectively against RF leakage, and 4) to make it easy to test, trouble-shoot and repair.

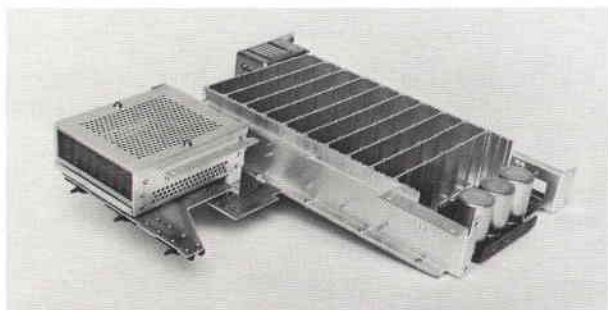
Essentially the entire instrument is assembled onto the main circuit board or 'motherboard'. Interlocking aluminum extrusion 'pockets' are mounted directly to the board. The major board assemblies plug into these pockets and become individually sealed modules. The front panel switch board assembly and counter box also plug directly into the motherboard as shown at left, below. The only hand wiring in the instrument is for the potentiometers on the front panel and the primary and secondary transformer windings.

Compatibility with the 8552/8553 Spectrum Analyzer has been accomplished by using the same panel color arrangement, similar panel trim and matching recessed dials for attenuation readout, as shown on page 11.

Effective RFI shielding has been achieved without reliance on expensive castings. Each major board assembly plugs into its own compartment on the motherboard. Each compartment is enclosed on its four sides by two closely-machined aluminum extrusions, on the top with a tight-fitting cast aluminum cover, and on the bottom by the ground plane on the motherboard. In some cases where high RF

attenuation is required, critical circuits have been installed in additional shielding cans inside their compartments. High-level RF signals are carried between modules in double-shielded coaxial cable. DC connections are made through the motherboard through small circular holes in the ground plane. In addition, the exposed leads and connector pins on the bottom side of the motherboard are shielded with a sheet aluminum cover. The counter box provides RF shielding of the low-frequency counter circuitry using overlapping riveted sheet metal and a unique metal etched screen in front to attenuate the RF radiating from the numeric indicator tubes. All this results in a unit well shielded against RFI susceptibility and radiation.

To achieve good serviceability all circuits are modularized and arranged in logical order in agreement with the instrument block diagram. Test points and signal paths are accessible so that a problem can be isolated to a single module without any disassembly other than removing the top cover. Then, with the removal of a few screws, a faulty module can easily be unplugged, removed and replaced. A fast factory module exchange program is being instituted for this product. Isolating problems below the module level is also simple. Extender boards are the only tools necessary to expose all circuit boards including the counter, for trouble-shooting under operating conditions, as shown at right, below.



A careful computer analysis of all the possible mixing products from each of the mixers was used to predict the amount of isolation necessary in the buffer amplifiers and to indicate the IF filtering necessary in the Tracking Generator to minimize spurious signals at the output. For example, mixing 3 MHz with 47 MHz in the first mixer in the Tracking Generator results in 50 MHz, but it also results in 44 MHz. If this signal were not prevented from returning to the Spectrum Analyzer through the 47-MHz LO line, it would mix with the 47 MHz and produce a spurious 3-MHz signal in the Analyzer IF. This same signal must also be filtered out in the Tracking Generator 50-MHz IF since otherwise it will appear as a spurious signal offset 6 MHz from the output signal. There can be many such spurious signals, some not nearly this obvious, in a triple conversion system with two swept

LO's. The computer analysis was a powerful aid in locating potential problems.

As noted in the discussion of the block diagram, the Tracking Generator output signal is kept at a constant level by an ALC circuit. Automatic leveling requires either an amplifier with a variable gain or a variable attenuator to adjust the RF level in response to the output detector. Such gain adjustments are simplest at a single frequency, but it is also desirable to have the input signal levels to the mixers remain constant to minimize spurious signals. Therefore, the 200-MHz IF amplifier was designed to have a voltage variable gain, since it operates at essentially a single frequency and it is the last element before the broadband third mixer. The gain is adjusted by placing a voltage tunable notch or trap between amplifier stages (see Fig. 4). As the ALC feedback voltage is

increased, the center frequency of the notch moves closer to 200 MHz, increasing the attenuation of the signal. This type of gain-adjusting element gives a range of more than 30 dB with a minimum of components.

ALC — Video Amplifier

The Tracking Generator provides a leveled output signal which is flat to ± 0.5 dB from 100 kHz to 110 MHz. The output level can be varied from +10 dB to -123 dBm with 1 and 10 dB step attenuators and a 0-1.2 dB gain vernier in the leveling circuit. Harmonics are more than 35 dB below the fundamental, while other spurious responses are more than 50 dB below the fundamental.

The Automatic Level Control circuit is shown in Fig. 5. The output level measured by the detector is compared with the reference voltage by the leveling amplifier, and the error signal from that amplifier is fed back to the variable-gain 200-MHz IF amplifier, as mentioned earlier. The major design objectives for the output circuitry of the 8443A were: 1) flat frequency response over the operating range, 2) a stable output level, 3) minimum level of spurious signals, 4) rapid recovery when sweeping through zero frequency.

Peak detection is used in the Tracking Generator because it has definite advantages over other diode detection schemes: it is accurate over a broad frequency range and stable over a broad temperature range; the output level of the 8443A varies less than ± 0.3 dB from 0 to 55°C. A peak detector is also simple, but it has one major problem: response to the rapid change in output power while sweeping through 'zero' frequency. This problem was solved by optimizing the dynamic input impedance of the leveling amplifier and limiting the charge on the detector filter capacitor due to the 'zero' frequency transient.

It was necessary to make some trade-offs in choosing the ALC loop gain to achieve optimum output signal flatness. Undesired mixing products from the RF Section can appear on the output as spurious signals. If the swept output signal crosses any of these signals, a zero beat or 'birdie' is produced on the signal when displayed on the Spectrum Analyzer. While these spurious signals have been minimized in the design of the RF Section, they are nonetheless multiplied by the amount of the loop gain in the ALC circuit. Therefore, it was necessary to make the unlevelled system as flat as possible, to minimize the amount of loop gain needed.

Thin-film microcircuit technology met the need for flat, high-gain output amplifiers. A high-gain amplifier is

required to give a high, level output, since the output of the third mixer is made low in level to minimize spurious signals. Flat frequency response is easier to achieve with a thin-film circuit because of its relative freedom from parasitic inductive and capacitive effects. Placing the detector on the thin-film circuit very close to the 50 Ω thin-film output resistor promotes the achievement of good VSWR characteristics in the leveled output. Microcircuit techniques are also advantageous because of the excellent heat sinking that is obtained by putting the active device directly on the sapphire substrate. This allows the active device to be biased at higher than normal current levels, which improves the overall frequency response of the transistors and minimizes the distortion in the output amplifier.

Counter Section

The 8443A marker control circuit stops the scan ramp generator in the 8552 IF Section during a part of each sweep cycle and counts the 8443A output frequency during the period when the scan is stopped and the frequency is fixed.

Because the scan is stopped at the same point on each sweep, the CRT beam is directed at the same point on the CRT for a large percentage of the scan time, causing an intensified spot at that point. This spot is an easily recognizable marker, and its position corresponds precisely to the frequency measured by the counter. By use of a continuously variable MARKER POSITION control, the operator can locate the marker on any point of the swept frequency display he chooses.

Obviously, it is necessary to stop the scan for a period sufficiently long to count the generator output to the desired resolution. For a direct counting counter, this period is simply the inverse of the desired frequency resolution. However, the intensity of the marker relative to the intensity of the rest of the scan is a function of the ratio of the

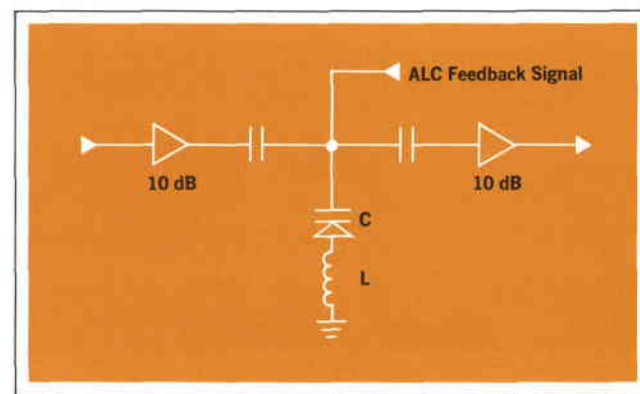


Fig. 4. Variable-gain 200-MHz IF Amplifier.

stopped period to the scanning period. As the operator changes either the counter resolution or the scan speed, the marker intensity will change. Since this characteristic is undesirable, a method was devised to minimize this effect. Given any resolution and scan speed, we can increase the marker intensity by stopping the scan for a period of time longer than the counting period, or we can decrease the intensity by blanking the CRT for a portion of the stopped time. The solution, then is to fix the ratio of the marker display time to the scan time at a value determined by the operator. This function is performed in the 8443A by a simple capacitor charge-discharge circuit.

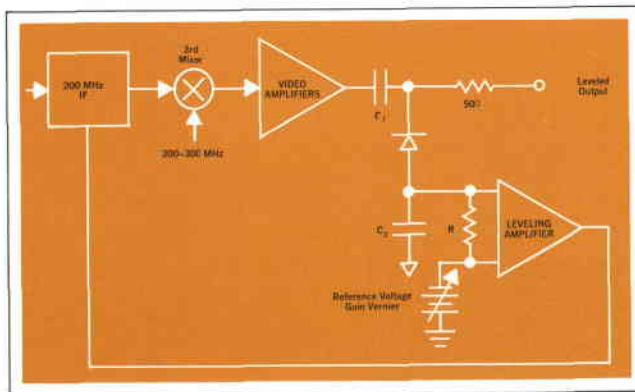


Fig. 5. Output Leveling System.

SYSTEM CHARACTERISTICS

HP Model 8443A*/8553B†/8552B‡

Spectrum Analyzer—Tracking Generator/Counter

FREQUENCY CHARACTERISTICS

FREQUENCY RANGE: 100 kHz to 110 MHz¹

SCAN WIDTH:

PER DIVISION: 18 calibrated scan widths from 20 Hz/div to 10 MHz/div in a 1, 2, 5 sequence on a 10 div display.

PRESET: 0 to 100 MHz.

ZERO: System is fixed tuned. Counter reads frequency.

DIGITAL FREQUENCY DISPLAY: Counter reads frequency of movable marker on CRT. 7 digits with 1 digit overrange. Reads to ± 10 Hz increments.

FREQUENCY ACCURACY:

COUNTER* ACCURACY: ± 1 count \pm time base accuracy.

Time Base Aging Rate: $< 3 \times 10^{-9}$ /day after warmup.

RESOLUTION:

BANDWIDTH: 3 dB bandwidths of 10 Hz \ddagger to 300 kHz provided in a 1, 3 sequence.

BANDWIDTH SELECTIVITY: 60 dB/3 dB IF bandwidth ratio

$< 11:1$ for IF bandwidths 10 Hz to 3 kHz

$< 20:1$ for IF bandwidth 10 kHz to 300 kHz.

STABILITY:

RESIDUAL FM:

Stabilized: < 0.1 Hz peak-to-peak typical. \ddagger

Unstabilized: < 1 kHz peak-to-peak.

NOISE SIDEBANDS: More than 70 dB below CW signal, 50 kHz or more away from signal, with 1 kHz IF bandwidth.

SPECTRAL PURITY:

HARMONIC SIGNALS: At least 35 dB below output level.

INHARMONIC (Spurious) SIGNALS: At least 50 dB below output level.

DISPLAY CHARACTERISTICS

SCAN TIME: 16 internal scan rates from 0.1 ms/div to 10 s/div in a 1, 2, 5 sequence. Scan hold mode allows manual scan.

DISPLAY OPTIONS: Spectrum analyzer is available with variable persistence (141T) or normal persistence (140T) and large screen (143S).

AMPLITUDE CHARACTERISTICS

ABSOLUTE AMPLITUDE CALIBRATION RANGE:

SPECTRUM ANALYZER:

Log: From -140 to $+10$ dBm, 10 dB/div on a 70 dB display or 2 dB/div expand below LOG reference.

Linear: From 0.1 μ V/div to 100 mV/div in a 1, 2 sequence on an 8-division display.

TRACKING GENERATOR: < -120 dBm to $+10$ dBm in 10 and 1 dB steps with a continuously adjustable 1.2 dB vernier.

MEASUREMENT RANGE:²

GAIN COMPRESSION: For < -10 dBm signal level at the input mixer, gain compression < 1 dB.

SPURIOUS RESPONSES: For -40 dBm signal level at the input mixer, spurious responses are more than 70 dB down (2 MHz–110 MHz).

AVERAGE NOISE LEVEL (1 MHz–110 MHz);

IF Bandwidth	Average Noise Level
10 Hz	-140 dBm

100 Hz	-130 dBm
1 kHz	-120 dBm
10 kHz	-110 dBm
100 kHz	-100 dBm

RESIDUAL RESPONSES (referred to signal level at input mixer):
200 kHz to 110 MHz: < -110 dBm

AMPLITUDE ACCURACY:

SPECTRUM ANALYZER:

Frequency Response: ± 0.5 dB

Switching between Bandwidths:³ ± 0.5 dB

Amplitude Display:⁴ ± 1.5 dB

Calibrator, -30 dBm at 30 MHz: ± 0.3 dB

TRACKING GENERATOR:

Frequency Response: ± 0.5 dB

Output Attenuators:

10 dB Steps: ± 0.2 dB

1 dB Steps: ± 0.1 dB

Calibrator, -30 dBm at 30 MHz: ± 0.3 dB

INPUT/OUTPUT CHARACTERISTICS

SPECTRUM ANALYZER:

INPUT IMPEDANCE: 50 Ω , Reflection Coefficient ≤ 0.13 (1.3 SWR) for input attenuator ≥ 10 dB.

MAXIMUM INPUT LEVEL: Peak or average power $+13$ dBm.

TRACKING GENERATOR:

OUTPUT IMPEDANCE: 50 Ω , Reflection Coefficient ≤ 0.09 (1.2 SWR) for output ≤ 0 dBm.

GENERAL

TEMPERATURE RANGE: Operation 0–55°C, storage -40 °C to 75°C.

POWER: 115 V and 230 V, 48–440 Hz (75 watts).

DIMENSIONS: Length, 18 $\frac{3}{8}$ in (466.7 mm); width, 16 $\frac{3}{8}$ in (425.4 mm); height, 3 $\frac{7}{8}$ in (98.4 mm), including height of feet.

WEIGHT: Net, 24 lb 5 oz (11.04 kg). Shipping, 31 lb 14 oz (14.47 kg).

PRICE (8443A* only): \$3500.00

8553B: \$2200.00

8552A: \$1900.00

8552B: \$2850.00

141T: \$1700.00

*Note availability of Model 8443B without counter, at \$1975.00

†Interfacing the 8443 Spectrum Analyzers with the earlier HP Model 8553L RF Section, a modification kit, will be required.

‡When the HP Model 8552A IF section is used, minimum bandwidth becomes 50 Hz, residual FM (in stabilized mode) is 20 Hz peak-to-peak. Only the newer 8552B IF section has the 2-dB LOG EXPAND display mode.

¹ The 8553B has a frequency range of 1 kHz to 110 MHz with two tuning ranges: 0–11 MHz and 0–110 MHz.

² Measurement range in the 'Frequency Response Mode' is determined by maximum signal level at the high end and the average noise level at the low end.

³ Error can be calibrated out by calibrating on specific bandwidth.

⁴ ± 0.25 dB/dB but not more than ± 1.5 dB over 70 dB display. Error can be calibrated out using IF substitution techniques. (Log Reference Level Control accuracy, 10 dB steps: ± 0.2 dB.)

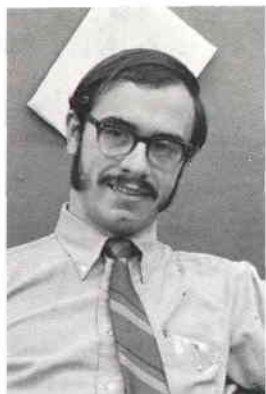
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Acknowledgments

The authors would like to acknowledge the contributions of Brian D. Unter, who was project leader during the early part of the design phase, Irving H. Hawley, who helped design several of the RF circuits, and Fred H.

Meyers, who assisted preparation of the instrument for release to production. Thanks are also due John R. Page, Jr., and Roderick Carlson for their encouragement and helpful suggestions during the project. 📷

Bob Hay



Pennsylvania-born Bob Hay took both his Bachelor's ('67) and Master's ('68) degrees in EE at Carnegie Tech. His option was systems. The summer before his last year he did circuit design at the Johns Hopkins Applied Physics lab. Bob joined HP straight out of Carnegie as a consequence of the company's college recruiting program. In his first post in the microwave division Bob took on circuit work for the 8443A. When this instrument

went into production he was promoted to project leader for a new program.

Bob and his wife, who met in college, are both after more education. He's pursuing an MBA at Santa Clara while she works toward her bachelor's in interior design at San Jose State. It leaves only a little time for some political activity and an occasional camping trip.

Pat Barrett



A native Californian, Pat Barrett took a general engineering degree from Harvey Mudd College, Claremont, in 1966, then went on to a Master's from Massachusetts Institute of Technology in '67. During that year he worked as a research assistant in the M.I.T. Instrumentation Lab.

In 1967 Pat joined the engineering program that led to the microwave division's 110-MHz spectrum analyzers, then went to work on the 8443A

project, becoming project leader when his predecessor was promoted.

Living in Palo Alto, Pat is married to a fellow Harvey Mudd graduate; she, too, holds an engineering degree and is employed as a technical editor. She shares Pat's creative interest in the graphic arts. Pat is a musician of better than average competence on the folk guitar.

Bill Bull



Bill Bull grew up in Menlo Park, California, put in three years at Dartmouth College in New Hampshire, worked a couple of years, then returned to college. He got a BS in mechanical engineering from San Jose State College (California) in 1965. Army Ordnance took him to Redstone Arsenal, White Sands, and Vietnam, where he earned a Bronze Star. He came out of the Army a captain in 1968 and was recruited soon thereafter by the HP microwave

division. His first assignment was product design of the 8443A.

Bill and his wife, whom he met at college, live in San Jose. They have a boy who has just passed his first birthday. Bill's mechanical abilities find another outlet in a 1940 Chevy that runs as no new one ever did.

Paul G. Winninghoff



Paul Winninghoff comes to us from Montana, at whose State College he took his BS in EE in 1962, and his Master's in the same discipline in 1963. He was elected there to Tau Beta Pi and Phi Kappa Phi. Upon graduation Paul put a year as a research associate at Montana State.

Paul's first project, upon coming to HP in 1964, was to design the log amplifier and the deflection circuits for the HP 110-MHz spectrum

analyzers. Since then he has done some work in microwave microelectronics, and was responsible for the power supplies, and ALC circuitry.

With all these activities, Paul still finds time to be an active radio amateur.

HEWLETT-PACKARD JOURNAL JULY 1970 Volume 21 • Number 11

TECHNICAL INFORMATION FROM THE LABORATORIES OF THE HEWLETT-PACKARD COMPANY PUBLISHED AT 1501 PAGE MILL ROAD, PALO ALTO, CALIFORNIA 94304
Editor: R. H. Snyder Editorial Board: R. P. Dolan, H. L. Roberts, L. D. Shergalis Art Director: Arvid A. Danielson Assistant: Maridel Jordan

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